

# Giovanni Agosta

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Born: December 28, 1975—Rome, Italy  
Nationality: Italian

## Current position

I currently hold the position of researcher with tenure at Politecnico di Milano, within the Dipartimento di Elettronica, Informazione e Bioingegneria. My research interests focus on the interaction between compiler and computer architecture, including compilation technologies for enforcing extra-functional properties such as performance, energy-efficiency, and security. Therefore, I participate in both the Advanced software architectures and methodologies and the System Architectures research lines within the Computer Science and Engineering section of the department. I am a founding member of the [HEAP Laboratory](#), where I lead a research team composed of two post-doctoral researchers, two doctoral students and four master's student.

## Research Vision Statement

Compiler technology is often considered a commodity, and therefore not at the forefront of research. While it is accurate to say that the field is mature, there is still a wide demand for better compilers, and a wide range of opportunities for major advances. In particular, commodity compilers only address to a marginal extent extra-functional properties of hardware/software systems other than performance. Indeed, important system properties such as energy efficiency and security are not satisfactorily addressed. *Thus, my primary research goal is to enlarge the range of extra-functional properties that can be optimized or enforced automatically through compiler transformations and analyses.*

### COMPILER TECHNIQUES FOR HARDENING CRYPTOGRAPHIC PRIMITIVES IMPLEMENTATIONS

An area where compilers can prove invaluable is that of protecting the software implementation of cryptographic primitives from attacks that exploit information leakage from side channels such as timing, power consumption, or electromagnetic emissions.

The precise quantification of information leakage is difficult to perform by hand, but, in collaboration with colleagues from the Applied Cryptography group (Prof. Gerardo Pelosi and Prof. Alessandro Barenghi), we were able to define a *Security-Oriented Dataflow Analysis* (SDFA) which can precisely identify, down to the individual bit level, which intermediate values of a computation are vulnerable to side channel analysis [C36, C40].

Based on the SDFA, it was then possible to define several protection strategies that can be applied automatically through the compiler [J12, C37, C38, C46], as well as some that employ self-modifying code as part of the defense [J11, C39]. Finally, to provide a full engineering approach, the SDFA was used as part of a secure-by-design methodology for the design of encryption solutions [J9, O3].

#### COMPILER TECHNIQUES FOR ENERGY EFFICIENCY & PERFORMANCE

Achieving energy efficiency through compiler transformations (and possibly through co-designing such transformations with the hardware architecture) is still an open problem for all kinds of computing systems, from embedded to high performance ones.

During the past years, I tackled several aspects of this problem, starting from the automated application and optimization of *memoization*, an approach to trade off memory space and computation time which is applicable to pure functions. Through a collaboration with the team led by Prof. Chiara Francalanci (Information Systems area), a compiler-based approach for Java applications was developed [J7, C26, O2].

A second line of work towards improving energy efficiency is that of compiler-architecture co-optimization [J2, J8]. I started the investigation on this topic by devising a method for modelling the performance impact of compiler and architecture parameters [J3], in collaboration with Prof. Cristina Silvano and Prof. Gianluca Palermo. Then, through a collaboration with the PULP team led by Prof. Luca Benini at ETH Zürich, we were able to co-design the compiler and the architecture of an OpenRISC core, with significant benefits [C49].

Recently, I started investigating compiler-based approaches to *approximate computing*, in the context of the H2020 ANTAREX project. In collaboration with the INRIA Rennes PACAP team, led by Dr. Erven Rohou, we obtained initial results on applying precision reduction to High Performance Computing (HPC) applications [C64], while with the Universidade do Porto team of Prof. João Cardoso we are working on applying precision tuning to heterogeneous architectures [C65].

#### DYNAMIC COMPILATION

Dynamic compilation is a key technique to exploit at compiler level runtime information. I have explored dynamic compilation techniques in conjunction with Very Long Instruction Word (VLIW) architectures [J1, C4, C8], providing VLIW scheduler designs for a Java Virtual Machine, under the supervision of Prof. Stefano Crespi Reghizzi. This research line led to the design of a Java Virtual Machine with a very small footprint for use in embedded devices [C9], as well as to the design of optimized selective compilation techniques (a.k.a. *hotspot*) [C7].

The study of the dynamic compilation process further led to the design of techniques for exploiting parallelism to hide compilation latencies, as well as to the implementation of such techniques in a dynamic compiler for Microsoft's CIL bytecode [J6, C19, C16, C25, O1].

More recently, with a doctoral student, Stefano Cherubin (2016-current), I revived this research line by investigating the applicability of partial dynamic compilation techniques in environments where dynamic compilers are not available or not desired for the entire application (e.g., HPC production environments) [J14].

#### REVERSE ENGINEERING

Reverse engineering is a key technique for malware and binary analysis as well as for legacy code support, via binary-to-binary translation. In this field I supervised a very successful doctoral student, Alessandro Di Federico (2015-current), whose work on fundamental techniques obtained good results through an innovative approach leveraging open source components such as QEMU and LLVM [C56]. This activity included a collaboration with Purdue University [C61], and resulted in an open source tool, REVAMB.

The current research direction along this line involves extending the ability of the reverse engineering tool to operate as a binary-to-binary compiler, in collaboration with a startup company, [Rev.ng srls Unipersonale](#).

#### PARALLEL PROGRAMMING MODELS & APPLICATIONS

Since automatic parallelisation is still far from effective, parallel programming models are key to achieving high performance, especially in heterogeneous systems. In collaboration with doctoral students and colleagues in the HEAP Laboratory, I co-designed one of the first solutions for parallel execution of the AES encryption primitive on CUDA-enabled General Purpose Graphics Processing Units (GPGPUs) [C20]. From this seminal work, we developed record-setting solutions for several encryption standards and security applications [C18, C22, C33, C34], and finally gathered the collected knowledge about the impact of architectural features on performance [J10].

Beyond the development of parallel applications, I also investigated the efficient implementation of programming models such as OpenCL [B2, C28, C47, C55, C23] and OpenMP [C30, C27]. Most recently, I designed and implemented a simple parallel programming model, the MANGO API, for use in High Performance Computing (HPC), characterised by the ability to integrate runtime-resource management. This programming model has been integrated with resource management techniques in collaboration with the research team of Prof. William Fornaciari [J15, C63, C57, O9]. This result integrates a series of ideas on resource management of parallel computing systems previously developed in collaborative research projects [C41, C44, C43, C62].

The current research direction along this line is to extend the programming model to provide support for predictability of performance in HPC systems, including performance portability across heterogeneous accelerators.

#### EMBEDDED & CYBER-PHYSICAL SYSTEMS DESIGN

While my interests revolve primarily around compiler technologies, I have been also involved in several research activities related to the design of embedded systems [B4, O6], including Internet of Things applications [J13, B5, O8] and cyber-physical systems [C45] (the latter in collaboration with the Human-Computer Interaction team led by Prof. Franca Garzotto), with an emphasis on the security aspects of such systems [C42, O4].

The current research direction along this line is focused on the application of secure and fast encryption techniques as well as of approximate computing strategies to specific embedded solutions.

#### ELECTRONIC DESIGN AUTOMATION

EDA tools and techniques are closely related to compilers. Therefore, there is often the opportunity to apply compiler technology to the analysis or synthesis of hardware specifications. In an early collaboration with Prof. Donatella Sciuto's group, I developed techniques for static analysis of transaction-level models [J4, C1], including UML-based modeling [B1] and adaptive metrics for functional partitioning [C10] (the latter in cooperation with Prof. Marco Santambrogio and with Prof. Seda Ogrenci Memik of Northwestern University).

With Prof. Francesco Bruschi and Prof. Gerardo Pelosi, we then provided a new insight, and related tools, on the nature of the *Boolean matching* problem in logic synthesis [J5, C14, C13].

## Habilitation for the position of Associate Professor

2017-2023

Settore concorsuale 01/B1, Informatica (Computer Science).

## Appointments held

- 2008-current Researcher with tenure, DEIB, Politecnico di Milano, Milano, Italy.
- 2005-2008 Researcher, DEI, Politecnico di Milano, Milano, Italy.
- 2004 Research Associate (Assegnista di Ricerca), DEI, Politecnico di Milano, Milano, Italy.  
Title of grant: "Compilazione e schedulazione dinamica per macchine VLIW" (Dynamic compilation and scheduling for VLIW architectures).
- 2001-2004 PhD Student, DEI, Politecnico di Milano, Milano, Italy.
- 1999-2000 Intern, Advanced Systems Technology group, STMicroelectronics, Agrate Brianza (MB), Italy.  
Assignment: design and implementation of an algorithm for parallelizing C code to be compiled for a cluster of ILP processors.

## Education

- 2004 PHD in Information Technology, Politecnico di Milano.  
Dissertation: "Dynamic Compilation for Architectures supporting Instruction Level Parallelism".  
Advisor: Prof. Stefano Crespi Reghizzi.
- 2000 LAUREA in Ingegneria Informatica (V.O.), Politecnico di Milano.  
Thesis: "Tecniche avanzate di compilazione applicate a macchine parallele e riconfigurabili" (Advanced Compilation Techniques for Parallel and Reconfigurable Architectures).  
Advisor: Prof. Stefano Crespi Reghizzi.  
Co-Advisor: Rinaldo Poluzzi, AST, STMicroelectronics.
- 1994 MATURITÀ CLASSICA, Liceo Ginnasio Giuseppe Parini, Milano.

## Honors & awards

I have been a member of the HiPEAC Network of Excellence since 2007, and have been awarded the "HiPEAC Paper Award" four times. The "HiPEAC Paper Award" is given in recognition of publications in top conferences in the Compilers and Computer Architectures areas, where the presence of European researchers is considered low. Furthermore, I have received two best paper awards, one of which from a conference sponsored by the ACM SIGAPP.

- 2015 "HiPEAC Paper Award" for the paper "Information leakage chaff: feeding red herrings to side channel attackers" appeared at DAC 2015.
- 2014 "HiPEAC Paper Award" for the paper "A Multiple Equivalent Execution Trace Approach to Secure Cryptographic Embedded Software" appeared at DAC 2012.
- 2014 Best Paper Awards (Overall and Cryptographic Techniques) at the SIN 2014 conference for the paper "Differential Fault Analysis for Block Ciphers: an Automated Conservative Analysis".
- 2013 "HiPEAC Paper Award" for the paper "Compiler-based side channel vulnerability analysis and optimized countermeasures application" appeared at DAC 2013.
- 2012 "HiPEAC Paper Award" for the paper "A code morphing methodology to automate power analysis countermeasures" appeared at DAC 2012.
- 2008 Best Paper Award (Applications area) at the ACM SAC 2008 conference for the paper "Dynamic Configuration of Application-Specific Implicit Instructions for Embedded Pipelined Processors".
- 2007-current Member of the [High Performance & Embedded Architectures and Compilers \(HiPEAC\) Network of Excellence](#).

## Research Activities

I have been involved in funded research projects since 2004, participating to 10 European projects, which obtained a total funding of over 36 M€, of which a total of over 4 M€ funded activities carried out by Politecnico di Milano. More specifically, activities directly managed by me, as Task leader, Workpackage leader, Project Technical Manager, or responsible for the local unit, accounted for a total funding of over 7.5 M€, of which over 1.8 M€ funding activities carried out by Politecnico di Milano.

Furthermore, as a Workpackage leader I managed activities involving at the same time up to 20 partners from all around Europe.

I have also been involved in the development of the project proposals for all the projects in which I have participated, except for ICODES, and have in particular been among the primary authors for the RECIPE, ANTAREX, and 2PARMA proposals.

The 2PARMA project was also deemed a *success story* by the European Commission.

### PARTICIPATION TO AND MANAGEMENT OF FUNDED RESEARCH PROJECTS

- 2018-current H2020 FET-HPC RECIPE  
Coordinator: Prof. William Fornaciari, Politecnico di Milano.  
Role: Project Technical Manager, responsible for all scientific and technical developments.  
Total EU contribution 3.28 M€, of which 0.705 M€ to Politecnico di Milano.  
EU contribution to managed activities: 3.28 M€, of which 0.705 M€ to Politecnico di Milano.
- 2016-current ECSEL JU [Safe Cooperating Cyber-Physical Systems \(SafeCOP\)](#), project id 100230.  
Coordinator: Detlef Scholle, Alten Sweden AB.  
Role: Task leader for Task 5.5, responsible for the vehicle-to-infrastructure for traffic management use case.  
Total EU contribution 3.78 M€, of which 0.125 M€ to Politecnico di Milano.  
EU contribution to managed tasks: 0.334 M€, of which 0.035 M€ to Politecnico di Milano.
- 2016-current H2020 ICT-04 [Modular Microserver DataCentre \(M2DC\)](#), project id 688201  
Coordinator: Dr. Ariel Oleksiak, Poznan National Supercomputing Center, Poland.  
Role: participant to Tasks 1.1 (Application Requirements) and T6.4 (Internet of Things Data Analytics).  
Total EU contribution: 8 M€ of which 0.25 M€ to Politecnico di Milano .
- 2015-current H2020 FET-HPC [AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems \(ANTAREX\)](#), project id: 671623.  
Coordinator: Prof. Cristina Silvano, Politecnico di Milano.  
Role: Task leader for Task 1.2, responsible for the specification of APIs and tools and T2.5, responsible for domain specific language features for extra-functional characteristics.  
Total EU contribution 3.11 M€ of which 0.577 M€ to Politecnico di Milano.  
EU contribution to managed tasks: 0.130 M€, of which 0.05 M€ to Politecnico di Milano.
- 2015-current H2020 FET-HPC [MANGO: exploring Manycore Architectures for Next-GeneratiOn HPC systems](#), project id 671668.  
Coordinator: Prof. José Flich Cardo, Universitat Politecnica de Valencia.  
Role: Workpackage leader for WP2, responsible for the software stack development including compilers, programming models, and runtime resource management.  
Total EU contribution: 5.8 M€, of which 0.646 M€ to Politecnico di Milano .  
EU contribution to managed workpackage: 1.1 M€, of which 0.331 M€ to Politecnico di Milano.

- 2015 EIT Digital Program 2015, Playful Supervised Smart Spaces (P3S).  
 Coordinator Prof. Franca Garzotto, Politecnico di Milano.  
 Role: Scientific responsibility for the local unit for Task A1501 (Smart Objects) responsible for the development of smart connected objects.  
 Total EIT contribution: 0.65 M€, of which 0.15 M€ to Politecnico di Milano. EIT contribution managed: 23 k€.
- 2010-2013 FP7-ICT [PARAllel PARadigms and Run-time MANagement techniques for Many-core Architectures \(2PARMA\)](#), project id 248716.  
 Coordinator: Prof. Cristina Silvano, Politecnico di Milano.  
 Role: Workpackage leader for WP2, responsible for compiler and OpenCL support development.  
 Total EU Contribution 2.741 M€ of which 0.545 M€ to Politecnico di Milano.  
 EU contribution to managed workpackage: 0.51 M€ of which 0.154 M€ to Politecnico di Milano.
- 2010-2013 ARTEMIS JU [Smart Multicore Embedded SYstems \(SMECY\)](#), project id 100230.  
 Coordinator: Dr. François Pacull, CEA LETI, France.  
 Role: Workpackage leader for WP3, responsible for the development of optimization techniques, programming model support, and fault tolerance.  
 Total EU contribution 3.27 M€, of which 0.25 M€ to Politecnico di Milano.  
 EU contribution to managed workpackage: 1.2 M€, of which 0.25 M€ to Politecnico di Milano.
- 2008-2009 FP7-ICT [OpenMediaPlatform](#), project id 214009.  
 Coordinator: Prof. Stefano Crespi Reghizzi, Politecnico di Milano.  
 Role: Workpackage leader for WP2, responsible for dynamic compiler development.  
 Total EU Contribution 3.27 M€ of which 0.545 M€ to Politecnico di Milano.  
 EU contribution to managed workpackage: 0.95 M€ of which 0.27 M€ to Politecnico di Milano.
- 2004-2007 FP6-IST [Interface- and Communication based Design of Embedded Systems](#), project id 004452.  
 Coordinator: Prof. Jens-E. Appel, OFFIS, Germany.  
 Role: Co-author of one deliverable on requirements on metrics for early communication cost estimation.  
 Total EU Contribution 2.85 M€, of which 0.27 M€ to Politecnico di Milano .

#### OTHER INTERNATIONAL COLLABORATIONS

In addition to international collaborations based on funded projects, I have also opened the following international research collaborations.

- 2016 Collaboration with Prof. Mathias Payer of Purdue University on reverse engineering techniques. One of the doctoral students under my supervision visited Purdue, resulting in a joint publication [C61].
- 2014 Development of compiler support and optimizations for the Open Hardware processor PULP, designed by ETH Zürich and Università degli Studi di Bologna. My team cooperated with the hardware design group led by Prof. Luca Benini, for an effective co-design of instruction set architecture and compiler [C49].

## Teaching and Supervision Activities

I have taught Compiler Construction courses at the graduate level since 2013, as well as a variety of courses at both the graduate and undergraduate level on algorithmics, system software design, and foundations of computer science. I have also taught a course on energy-aware computing within the doctoral program in Information Technology.

I have been advisor of two doctoral students, co-advisor of three, and I am currently supervising two more.

I am also supervising the research activities of two post-doctoral research associates, and have co-supervised another.

### SUPERVISION OF POST-DOCTORAL RESEARCH ACTIVITIES

- 2018-current Supervisor of post-doctoral research activities ("assegno di ricerca") for dr. Alessandro Di Federico.
- 2018-current Supervisor of post-doctoral research activities ("assegno di ricerca") for dr. Pietro Fezzardi.
- 2013-2015 Co-supervisor (with Prof. Luca Breveglieri) of post-doctoral research activities ("assegno di ricerca") for dr. Alessandro Barenghi.

### SUPERVISION OF DOCTORAL AND MASTER'S STUDIES

- 2017-current Advisor for the doctoral studies of Anna Pupykina, PhD program in Information Technology, XXXII cycle, Politecnico di Milano.  
Topic of research: Resource management of deeply heterogeneous HPC systems.
- 2016-current Advisor for the doctoral studies of Stefano Cherubin, PhD program in Information Technology, XXXI cycle, Politecnico di Milano.  
Topic of research: Approximate computing for HPC and Embedded Systems.
- 2015-2017 Advisor for the doctoral studies of dr. Alessandro Di Federico, PhD in Information Technology, XXX cycle, Politecnico di Milano.  
Title of dissertation: "Compiler Techniques for Binary Analysis and Hardening".  
First employment after achieving the doctoral degree: Research Associate at Politecnico di Milano.
- 2013-2015 Advisor for the doctoral studies of dr. Michele Scandale, PhD in Information Technology, XXVIII cycle, Politecnico di Milano.  
Title of dissertation: "Towards Improving Programmability of Heterogeneous Parallel Architectures".  
First employment after achieving the doctoral degree: Compiler Engineer at Apple.
- 2011-2013 Co-Advisor of the doctoral studies of dr. Marco Bessi (Advisor: Prof. Chiara Francalanci), PhD in Information Technology, XXVI cycle, Politecnico di Milano.  
Title of Dissertation: "A Methodology to Improve the Energy Efficiency of Software"  
First employment after achieving the doctoral degree: Solution Delivery Consultant at CAST.
- 2010-2012 Co-Advisor of the doctoral studies of dr. Ettore Speziale (Advisor: Prof. Stefano Crespi Reghizzi), PhD in Information Technology, XXV cycle, Politecnico di Milano.  
Title of Dissertation: "Improving Synchronization and Data Access in Parallel Programming Models".  
First employment after achieving the doctoral degree: Compiler Engineer at ARM Ltd.
- 2008-2012 Co-Advisor of the doctoral studies of dr. Andrea Di Biagio, PhD in Information Technology, XXIII cycle, Politecnico di Milano (Advisor: Prof. Stefano Crespi Reghizzi).  
Title of Dissertation: "Synchronization Optimization for Distributed Shared Memory Multiprocessors".  
First employment after achieving the doctoral degree: Compiler Engineer at Sony SN Systems.
- 2004-current Advisor of theses for the degree of Master of Science in Computer Engineering at Politecnico di Milano (10 in the last 5 years).

2003 Mentor for the Master of Engineering in Embedded Systems Design thesis of Prasad Balasubramanian, "Impact of source code specialization on energy and performance of software", Advanced Learning and Research Institute, Università della Svizzera Italiana, Lugano (CH).

#### MEMBERSHIP IN REVISION COMMITTEES FOR DOCTORAL CANDIDATES

2016-current Member of revision committee (external examiner) for the doctoral studies of Pedro Miguel dos Santos Pinto, at Faculty of Engineering of the University of Porto, Portugal.

2007 Member of revision committee (controrelatore) for the doctoral studies of Alberto Gallini, at Università di Milano Bicocca.

#### COURSES

2018 "Introduzione alla programmazione in Python" (introduction to programming in Python), within the extra-curricular innovative teaching program for Engineering students at Politecnico di Milano (all levels from undergraduates to doctoral students), in collaboration with Dr. Francesco Bruschi.

2016 "Energy aware design of computing systems and applications", within the doctoral program in Information Technology at Politecnico di Milano, as the primary organizer (with Prof. William Fornaciari as co-organizer).

2014 "Energy aware design of computing systems and applications", within the doctoral program in Information Technology at Politecnico di Milano, as a co-organizer with Prof. William Fornaciari.

2013-current Code Transformation and Optimization, within the Master of Science in Computer Engineering (Laurea Specialistica in Ingegneria Informatica) at Politecnico di Milano.

2012 The zPARMA OpenCL Compiler Toolchain, at the Fall School on Programming Paradigms for Multicore Embedded Systems, Oct 2012, Freudenstadt, Germany (with Michele Scandale).

2011-2012 Piattaforme Software per la Rete (software platforms for networking) within the Laurea in Ingegneria Informatica and Laurea in Ingegneria delle Telecomunicazioni (Computer Engineering and Telecommunications Engineering, undergraduate programs) at Politecnico di Milano.

2010 Algoritmi e Principi dell'Informatica (principles of algorithms and data structures) within the Laurea in Ingegneria Informatica (Computer Engineering, undergraduate program) at Politecnico di Milano.

2007-2010 Informatica 3 (principles of programming language design, algorithms and data structures) within the Laurea in Ingegneria Informatica (Computer Engineering, undergraduate program) at Politecnico di Milano.

2005-2010 Laboratorio Software (software design and operating systems laboratory) within the Laurea Specialistica in Ingegneria Informatica (Computer Engineering, graduate program) at Politecnico di Milano.

2004 Informatica C (fundamentals of computer programming and architecture) within the Laurea in Ingegneria Chimica e dei Materiali (Chemical Engineering, undergraduate program) at Politecnico di Milano.

#### OTHER TEACHING ACTIVITIES

2001-current Teaching Assistant at Politecnico di Milano for the courses of foundations of computer science (undergraduate programs in Computer Engineering, Telecommunication Engineering, Mathematical Engineering, and Chemistry and Materials Sciences).

2013-current Teaching Assistant at Politecnico di Milano for the courses of Advanced Computer Architectures (graduate program in Computer Engineering).



- 2002-2006 Teaching Assistant at Politecnico di Milano for the courses of High Performance Processors (graduate program in Computer Engineering in conjunction with University of Illinois at Chicago).
- 2002-2007 Teaching Assistant at Politecnico di Milano for the courses of Formal Languages and Compilers (graduate program in Computer Engineering).

## Service Activities

### ORGANISATION OF SCIENTIFIC CONFERENCES AND WORKSHOPS

- 2018 Member of the program committee for the [IFIP International Conference on New Technologies, Mobility & Security \(NTMS 2108\)](#).
- 2018 Member of the program committee for the [14th International Workshop on Scheduling and Resource Management for Parallel and Distributed Systems \(SRMPDS2018\)](#).
- 2017 Member of the program committee for the [1st Workshop on Autotuning and Adaptivity Approaches for Energy Efficient Systems \(ANDARE\)](#), held in conjunction with the 26th International Conference on Parallel Architectures and Compilation Techniques (PACT).
- 2016-current Member of the program committee of the [International Workshop on High Performance Energy Efficient Embedded Systems \(HiP3ES\)](#).
- 2016-current Member of the program committee for the [Design Automation and Test in Europe \(DATE\)](#), Special Track on EU Projects.
- 2015-current Member of the program committee of the Euromicro Conference on Digital System Design, for the [Special Session on Architectures and Hardware for Security Applications](#).
- 2015 Member of the program committee of the [International Workshop on Architecture-Aware Simulation and Computing](#).
- 2014-current Member of the organizing and program committee of the [Workshop on Cryptography and Security in Computing Systems \(CS<sup>2</sup>\)](#), co-located with the HiPEAC Conference (founding member). The proceedings of the CS<sup>2</sup> workshop are published in the ACM International Conference Proceedings Series.
- 2014-current Member of the program committee of the [International Conference on Embedded Computing Systems: Architectures, Modeling and Simulation \(SAMOS XVI\)](#).
- 2011 Finance Chair for the [Architecture of Computing Systems \(ARCS 2011\)](#) conference.
- 2010-current Member of the organising and program committees for the [Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures \(PARMA\)](#) (founding member) and of the [Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms \(DITAM\)](#) (starting from the third edition, held jointly with the PARMA workshop), co-located with the HiPEAC Conference (and, for the 1st and 2nd PARMA Workshop only, with the ARCS conference).  
Program Chair in 2016 and 2017.  
General Chair in 2015.  
The proceedings of the PARMA-DITAM workshop are published in the ACM International Conference Proceedings Series.
- 2008 Local arrangements Co-Chair for the [41st IEEE/ACM MICRO Conference](#).

### REVISION OF SCIENTIFIC ARTICLES AND PROJECT PROPOSALS

- 2017 Rapporteur (responsible for the consensus report) and reviewer for the COST (European Cooperation in Science and Technology) Association Open Call OC-2016-2.
- 2015 Reviewer for two project proposals for the 1/2016 Academic Research Fund Tier 2 Grant Call MOE2015-T2-2 of the Singapore Ministry of Education.
- 2011 Evaluator for the CHIST-ERA (European Coordinated Research on Long-term Challenges in Infor-

mation and Communication Sciences & Technologies) Call 2011.

2010-current

Reviewer of scientific articles for several international journals, including: ACM Transactions on Architectures and Code Optimization; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Microprocessors and Microsystems (Elsevier); IEEE Transactions on Computers.

#### OTHER SERVICE ACTIVITIES

2016-current

Mentoring of student teams to the ACM International Collegiate Programming Competition.

2011-current

Member of the logistics board of the School of Industrial and Computer Engineering, Politecnico di Milano.

2001-2002

Elected representative of the doctoral students to the Department council of DEIB, Politecnico di Milano.

## Publications & Talks

I have published a total of 14 articles in scientific journals with international peer-review committees (plus one accepted pending minor revision), as well as 4 book chapters (plus one in print) and 65 papers in conferences and workshops with international peer-review committees.

Finally, I have also held three invited talks, one at the 18th IEEE Conference on Computational Science and Engineering, and two at the HiPEAC Virtualization Cluster Meeting.

#### Bibliometrics:

**Google Scholar** citations 661, h-index 15

**Scopus** citations 383, h-index 11

According to SciVal<sup>1</sup>, for the last five years, my publications have a field-weighted citation impact of 1.67 (i.e., are cited 67% more than expected for the research area). For my overall career, the same metric is 1.48, indicating that my publications have achieved an increased impact in the last years.

Considering recent publications, over 35% have been authored in collaboration with international partners, and over 18% included an industrial collaboration, including companies such as Thales Communications & Security, ARM Ltd, Philips HealthTech, STMicroelectronics, Synopsys, Vodafone Automotive, Dompé Farmaceutici, Eaton Industries, Alten.

#### INTERNATIONAL JOURNAL ARTICLES

[J1] G. Agosta, S.C. Reghizzi, G. Falauto, and M. Sykora. JIST: Just-In-Time scheduling translation for parallel processors. *Scientific Programming*, 13(3):239–253, 2005.

[J2] Giovanni Agosta, Luca Breveglieri, Gerardo Pelosi, and Martino Sykora. Programming Highly Parallel Reconfigurable Architectures for Symmetric and Asymmetric Cryptographic Applications. *Journal of Computers*, 2(9):50–59, 2007.

[J3] Cristina Silvano, Giovanni Agosta, and Gianluca Palermo. Efficient architecture/compiler co-exploration using analytical models. *Design Automation for Embedded Systems*, 11(1):1–23, 2007.

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<sup>1</sup>SciVal is Elsevier research intelligence tool. The metrics provided are computed on Scopus data.

- [J4] Giovanni Agosta, Francesco Bruschi, and Donatella Sciuto. Static analysis of transaction-level communication models. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(8):1412–1424, 2008.
- [J5] Giovanni Agosta, Francesco Bruschi, Gerardo Pelosi, and Donatella Sciuto. A transform-parametric approach to boolean matching. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 28(6):805–817, 2009.
- [J6] Simone Campanoni, Giovanni Agosta, Stefano Crespi Reghizzi, and Andrea Di Biagio. A highly flexible, parallel virtual machine: design and experience of ILDJIT. *Software: Practice and Experience*, 40(2):177–207, 2010.
- [J7] Giovanni Agosta, Marco Bessi, Eugenio Capra, and Chiara Francalanci. Automatic memoization for energy efficiency in financial applications. *Sustainable Computing: Informatics and Systems*, 2(2):105–115, 2012.
- [J8] Andrea Di Biagio, Giovanni Agosta, Martino Sykora, and Cristina Silvano. Architecture optimization of application-specific implicit instructions. *ACM Transactions on Embedded Computing Systems (TECS)*, 11(SUPPL. 2), 2012.
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## OTHER PUBLICATIONS

I have also co-authored and/or edited a number of technical works, including technical reports to the European Commission, most of which are not reported for the sake of brevity. Herebelow I report a selection of the most relevant and recent invited papers, posters, editorials, and publications in technical magazines.

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- [O9] Federico Reghenzani, Giuseppe Massari, Anna Pupykina, Giovanni Agosta, and William Fornaciari. Resource and memory management in MANGO heterogeneous system. HiPEAC Summer School Posters, 2017.

- [O10] Cristina Silvano, Andrea Bartolini, Andrea Beccari, Candida Manelfi, Carlo Cavazzoni, Davide Gadioli, Erven Rohou, Gianluca Palermo, Giovanni Agosta, Jan Martinovič, et al. The ANTAREX Tool Flow for Monitoring and Autotuning Energy Efficient HPC Systems (Invited paper). In *SAMOS 2017-International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation*, 2017.
- [O11] Giovanni Agosta, Alessandro Barenghi, Israel Koren, and Gerardo Pelosi, editors. *CS2 '15: Proceedings of the Second Workshop on Cryptography and Security in Computing Systems*, New York, NY, USA, 2015. ACM.
- [O12] Giovanni Agosta, Alessandro Barenghi, Israel Koren, and Gerardo Pelosi, editors. *CS2 '16: Proceedings of the Third Workshop on Cryptography and Security in Computing Systems*, New York, NY, USA, 2016. ACM.
- [O13] Giovanni Agosta, Alessandro Barenghi, and Gerardo Pelosi, editors. *CS2 '17: Proceedings of the Fourth Workshop on Cryptography and Security in Computing Systems*, New York, NY, USA, 2017. ACM.
- [O14] Giovanni Agosta, Cristina Silvano, João Cardoso, and Michael Huebner, editors. *PARMA-DITAM '15: Proceedings of the 6th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures*, New York, NY, USA, 2015. ACM.
- [O15] Cristina Silvano, João Cardoso, Giovanni Agosta, and Michael Huebner, editors. *PARMA-DITAM '16: Proceedings of the 7th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 5th Workshop on Design Tools and Architectures For Multicore Embedded Computing Platforms*, New York, NY, USA, 2016. ACM.

#### INVITED TALKS

- 2015 G. Agosta. "The MANGO FET-HPC Project: An Overview", held at 18th IEEE Conference on Computational Science and Engineering, Special Session on FET-HPC and Exascale Recently EU-Funded Projects, Porto (Portugal), October 2015.
- 2010 G. Agosta, "Application Virtualization: The 2PARMA Approach", held at HiPEAC Virtualization Cluster Meeting, October 2010, Barcelona, Spain.
- 2010 G. Agosta, "The 2PARMA Compiler Toolchain", held at HiPEAC Compilation Cluster Meeting, October 2010, Barcelona, Spain.

#### SOFTWARE

I have supervised and participated to the development of numerous software packages. I report here only the major packages for which I either had a primary design role, or coordinated a development team across multiple years.

- 2017-current MANGOLIBS, a parallel programming model for deeply heterogeneous architectures integrating resource management.  
Role: scientific leadership, design and implementation of the first two versions [C63] (the current version is co-developed with Federico Reghenzani and Anna Pupykina).
- 2016-current LIBVERSIONINGCOMPILER, a library for easy dynamic code versioning and specialization.  
Role: scientific leadership, design and implementation of the first version (superseded by the current version [J14], developed by Stefano Cherubin).

- 2012-current OPENCRUN, an implementation of the OpenCL programming model [C43].  
Role: scientific leadership (design and development by Ettore Speziale, Michele Scandale, and Giulio Sichel).
- 2012 CODE MORPHING ENGINE, a polymorphic engine for the generation of semantically equivalent code fragments employed in protecting the software implementation of cryptographic primitives against side channel attacks [C32].  
Role: scientific co-leadership, design and implementation (co-leadership by Gerardo Pelosi).
- 2001-2005 JIST, a just-in-time compiler for VLIW architectures featuring efficient instruction scheduling [C4, J1].  
Role: scientific leadership, design (developed primarily by Martino Sykora and Gerlando Falauto).

I authorize the treatment of personal data according to the privacy regulations of D.Lgs. n. 196/2003, "Codice in materia di protezione dei dati personali", and subsequent modifications.

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