Abstract
Embedded systems can be considered as specialized computing systems which can be used for multi-purpose application varying from mobile-phone to military and home-automation devices. Although the functionalities of these devices are differed, the computational structure and design is tightly connected with the platform and programmability in which they rely on.

During this design phase, Design Space Exploration (DSE) plays a major role to benefit the designer, to prune the large design space and support the designer during the analysis phase. For addressing the complex solution space, there is a necessity to extend conventional exploration approaches by applying data-mining for extract knowledge from statistical results.

The goal of this work is to develop statistical exploration and analysis framework for the compiler-architecture co-design in VLIW processors to tackle the aforementioned problem by proposing an automatic methodology based on a tool-chain including the MOST tool (Multi-Objective System Tuner) for managing the DoE and generating the configurations; LLVM compiler for implementing the explored compiler sequences and source to source transformations; the VEX compiler simulator for mapping and evaluating the different program instances onto VLIW architecture and R statistical language for data analysis.

The proposed framework could be used for analyzing the compiler options, combined with the architectural parameters. Thus, we provide the designer an integrated environment to automatically explore, and analyze code transformation sequences enabling compiler auto-tuning. We expect that the knowledge extracted from the proposed framework will be further used to eventually provide useful hints for deciding promising ordering of compiler transformations.

References
Design Space Exploration and Analysis of Compiler Transformations on VLIW Processors

Motivation
- Complex Solution Space
- Data-mining: Extract knowledge from statistical data (application patterns, effect, etc)
  - A multi-objective optimization problem
  - Maximize the performance of the platform
  - Minimize the power consumption
  - Minimize other non-functional metrics

General View

Exploration and Analysis Framework

Problem
Huge set of design space and affecting parameters

Goals
Automatically explore the design space and analyze the compiler-architecture co-design in VLIW processors
Introducing a new automatic tool-chain methodology by applying customized random design of experiment algorithm

Tools
1. MOST tool (Multi-Objective System Tuner)
2. Two open-source compilers; LLVM and VEX
3. R statistical Language
4. Several standard benchmarks for both embedded and high performance domain

Analysis Results and Future Work

GSM Analysis Results

Future Work
1. Combining Architectural Parameters
2. Extended to target Phase Ordering
3. Utilize results to drive optimizations