Cristiana Bolchini

Date of birth	December 11, 1968
Languages	Italian (native), English (fluent)
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Main facts

- Multidisciplinary research interests covering two different areas: Embedded System Design and Design Methodologies for Dependable Computing in the Computer Architecture area, and Context-Aware Data Design and Management within the Pervasive Database area. The former research topic is the mainstream one, carried out since the graduating thesis, building a solid experience on dependability-related issues in the design of embedded/computing systems. The latter has been pursued in the last decade, contributing to develop an innovative research trend on context-awareness. Active participation to research in both areas has led to involvement in EU/Italian projects and to several high-level publications in both fields (selected publications are evenly balanced between both areas).
- Coordinator of the *FP7 STREP project SAVE* (Sep. 2013 - Aug. 2016), on "Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures" ◇ Proponent & MC member for Italy of *EU COST Action MEDIAN* – "ManufacturablE and Dependable multIcore Architectures at Nanoscale" (Dec. 2011 - Nov. 2015) ◇ Recipient of two US$ 100,000 *gifts* from *Cisco University Research Program Fund* of Silicon Valley Community Foundation (Dec. 2012, Oct. 2014) ◇ co-PI for Politecnico di Milano for project "Zero Energy Buildings in Smart Urban Districts" (National Technological Cluster on "Technologies for Smart Communities") (2014 - 2017) ◇ co-PI for Politecnico di Milano for project "SCUOLA - Smart Campus as Urban Open LAbs" (Regione Lombardia, area "Smart Cities and Communities") (2014 - 2015) ◇ Local PI for *PRIN 2008* on "High reliability fault tolerant digital systems in nanometric technologies: characterization and design methodologies" ◇ Participant to several other EU/industrial funded projects.
- Three papers in the IEEE Trans. on Computers among the 14 journal publications of the last 6 years. In total, 130+ peer-reviewed papers in international journals (10 IEEE/ACM journals) and conferences/symposia.
  h-index: 23 ◇ Total citations: 2040 ◇ academic age: 24 yrs (src: Google Scholar, June 2017)
- Starting in 1997, 2+ courses taught per academic year: Computer Science Fundamentals (Undergraduate course: 160+ students) since 1997, Digital logic design (Undergraduate course: 120+ students) since 2005, Dependable Systems (Graduate/PhD course: ~20 students) since 2005 (except 2008).
- Associate Editors-in-Chief of the *IEEE Trans. on Emerging Topics in Computing* (2013 - 2015), Associate Editor for the *IEEE Trans. on Computers* (2007 - 2012), and Guest Editor for special issues on dependability-related topics for Springer and Elsevier journals, IEEE Trans. on Computers and IEEE Trans. on Nanotechnology.
- Track Chair for the Test Track for Date 2018, Program Co-Chair for Track T4 - On-Line Test, Fault Tolerance and Robust Systems for DATE, 2015, 2016, Chair of the Tutorials for DATE 2016, 2017, Program Co-Chair for the Friday Workshops for DATE 2013, 2014 and 2015, General and Program co-chair of the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems (2002, 2003, 2007 and 2008). Serving on several Technical Program Committees of conferences/symposia on reliability-related topics (including ICCAD, DAC, DATE, DFT).
- At present, supervising 1 PhD student; advisor of 3 PhD students, 4 Research Assistants in the past, supervised internal and foreign students for their graduating thesis.
- Academic responsibilities/services: member of the Computer Science section board (since 2013), vice-head of the PhD board in Information Technology for the Computer Science section (since 2016), member of the committee for National Scientific Qualification for the area/section 09/H1 (since Nov. 2016) and delegate for international relationship with the Far East Asia - Engineering (since June 2017).

Contents

1 Profile

Cristiana Bolchini's scientific profile is two-fold, as she started her research career in the Computer Architecture group at the Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB) of Politecnico di Milano, working within the field of Embedded System Design and Design Methodologies, and a decade later also extended her interests in the Database, Web and Society group of the same department, contributing to the Context-Aware Data Design and Management area.

Cristiana Bolchini started working in the Dependable Computing Systems area during her graduating thesis, partially developed under the umbrella of a funded stage at the Italtel research laboratories, with the aim of defining an expert system able to support ASIC designers in the implementation of easy-to-test devices by means of an automatic application of Design-for-Testability (DfT) techniques. The research, supervised by Prof. Donatella Sciuto, was part of a European funded Esprit project, PATRICIA, involving both Politecnico di Milano and Italtel. In the following years, Cristiana's effort focused on other dependability issues in the design of embedded systems, mainly related to the definition of methodologies and tools for designing, implementing and analysing digital systems able to autonomously detect the occurrence of hardware faults and possibly tolerate their effects, targeting different kinds of architectures, platforms and abstraction levels, always keeping into consideration state-of-the-art and future technologies. The products of these years are 15+ papers published in peer-reviewed journals and magazines (five IEEE Transactions, plus Elsevier and Springer journals), 70+ papers presented at international conferences and symposia and software tools to support the designers in the introduction of fault detection/tolerance mechanisms, and the analysis of the achieved reliability characteristics. Based on her expertise, she has been involved in several technical program committees of conferences (e.g., DATE, DAC, DFT, ICCAD), and has been the Program Co-Chair and General Co-Chair in four different editions of the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems (DFT). Starting with the PATRICIA project, she has been involved in several research projects, contributing on the aspects specifically devoted to dependability issues. During the years Cristiana has built a network of national and international relationships at the basis of two projects she has been directly in charge of: at the national level, MIUR PRIN 2008 project, "High reliability fault tolerant digital systems in nanometric technologies: characterization and design methodologies" (local Principal Investigator), at the international level she has been one of the five proponents of the EU COST Action "Manufacturable and Dependable Multicore Architectures at Nanoscale" (MEDIAN, 2011-2015).

While in the past this area of research was mainly attractive for highly (safety) critical environments (e.g., space and health), today dependability has become a major challenge also for traditional contexts, because of the pervasiveness of embedded/computing systems, such that the correctness of operation even in presence of faults is paramount. Indeed, systems, requirements, constraints, costs and the whole context are continuously changing, however Cristiana's experience and expertise built during the past decades offers a solid basis for up taking the new challenges.

Cristiana's present research and professional interests are centered on the development of dependable systems by means of new software/hardware technologies for runtime adaptation to mitigate the effects of failures and lifetime improvement. This focus is extended to support the dynamic management of the tradeoff between dependability, performance and energy, to offer adaptive mechanisms suitable for a broad spectrum of computing scenarios. Runtime adaptation and the mentioned tradeoffs are the innovative contributions expected from the new EU FP7 STREP project she is coordinating, "Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures" (SAVE, 2013-2016), where Politecnico is also responsible of the self-adaptiveness major challenge. Adaptiveness is also the key for another ongoing research within the dependability field, related to functional diagnosis. The interest, begun as an industrial collaboration with Cisco Systems, has flourished in a broader scenario with novel solutions based on the exploitation of data mining as a reasoning based mechanism to incrementally and adaptively drive engineers during the diagnosis of faulty complex boards. A US$100,000 *gift* has been awarded to Cristiana in Dec. 2012 to carry out her research in the field, from the Cisco University Research Program Fund of Silicon Valley Community Foundation. Given the positive results of this first research, a second *gift* (US$100,000 in Oct. 2014) has been awarded from the same foundation to continue the research in project "FIND^2: A flexible functional diagnosis framework based on machine-learning techniques".

Context-awareness in data design and management is the research area at DEIB stemming from the collaboration with Prof. Letizia Tanca and Prof. Fabio A. Schreiber, in the early 2000s, focused on the emerging challenges related to data access in mobile devises, characterised by – at the time – limited resources. Context-awareness has been identified as the key to deal with the large amount of data to be dynamically tailored for the specific user and his/her contexts in order to reduce the quantity of data to be used without information loss. The research has received a lot of attention (258 citations for a survey published on the ACM Sigmod Record in 2007) and the outcomes are 11 papers published in high-ranking journals and magazines (i.e., Elsevier's Information Systems, Communications of the ACM), a number of paper presented at conferences (including an invited contribution and a special extended talk) and three book chapters reporting the major outcomes of two important MIUR FIRB projects – MAIS and ART-DECO –. The MIUR PRIN 2005 Project "Emergent Semantics and cooperaTion in multi-knowledgE EnvironMents" (ESTEEM) offered a great context to spin the research (two joint publications in important journals present the overall view of the outcomes), subsequently exploited in the more recent ERC project "Self-Managing Situational Computing".

Besides continuing along these lines, Cristiana's current contribution is towards the adoption of the same rigorous approach developed within this research field in the computing/embedded system design scenario, for self-adaptive, context-aware system model and design, thus bridging the two research areas.

As a new recent involvement, Cristiana Bolchini is contributing to two projects started in 2014, namely a project on "Zero Energy Buildings in Smart Urban Districts" (National Technological Cluster on "Technologies for Smart Communities") and another on "SCUOLA - Smart Campus as Urban Open LAbs" (Regione Lombardia, area "Smart Cities and Communities"), in close collaboration with colleagues of other research areas of the same institution (e.g., Architecture, Built Environment and Construction Engineering, Systems and Control, and Telecommunication) for the exploitation of ICT solutions for the development of smart buildings and districts to improve energy efficiency through optimised used of resources and users' awareness.

2 Position and Education

Record of Employment

Mar. 2015 – present	Full Professor at Politecnico di Milano, (School of Industrial and Information Engineering), Scientific Area: 09/H1.
Dec. 2003 – Mar. 2015	Associate Professor at Politecnico di Milano, (School of Industrial and Information Engineering), Scientific Area: 09/H1. *Confirmed since Dec. 2006.*
Sep. 1999 – Dec. 2003	Assistant Professor at Politecnico di Milano, (V School of Engineering), Scientific Area: "Computer Engineering".
Mar. 1999 – Sep. 1999	Consultant on design methodologies and reliability issues – Politecnico di Milano, DEI.
Feb. 1998 – Jan. 1999	Scholarship for research on "Quality-driven digital system design methodologies" (12 months) – CNR
1997 – 1998	Scholarship for research on "ASIC design and formal verification" (8 months). – Politecnico di Torino
Nov. 1993 – Nov. 1996	Ph.D. in Computer Science and Automation Engineering at Politecnico di Milano, DEI.
Feb. 1993 – Nov. 1993	Consultant for projects related to design-for-testability issues, starting from VHDL specifications – Politecnico di Milano, DEI.

Education

Dec. 2013	National Scientific Qualification (valid until 03/12/2017) as a full professor (SSD: 09/H1)
Nov. 1993 – Nov. 1996	Ph.D. in Computer Science and Automation Engineering Politecnico di Milano, Dipartimento di Elettronica e Informazione Thesis: *Quality issues in the design of digital systems* Advisor: Prof. D. Sciuto
May 1993	Italian Professional Qualification for Engineers (Esame di Stato per l'abilitazione alla Professione di Ingegnere)
Oct. 1987 – Feb. 1993	Laurea in Electronic Engineering (5 years course, equivalent to B.Sc and M.Sc) Thesis: *A support system for the design of easily testable VLSI architectures: design and implementation of an expert system for the application of Design-for-Testability techniques* Advisor: Prof. M. G. Sami Grade: 98/100
Sep. 1982 – Jun. 1987	Scientific high school diploma from Galileo Galilei in Caravaggio (grade: 54/60)
Aug. 1985 – Jun. 1986	High School diploma from Mount Vernon High School, in Mount Vernon, MO, U.S.A.

Scholarships

- Scholarship from CNR (1998 – 1999).
- Scholarship from Politecnico di Torino (1997 – 1998).
- Stage with scholarship at ITALTEL-SIT while working on the M.Sc. graduation thesis (June 1992 – Feb. 1993).

3 Fields of interest

Cristiana Bolchini's research interests fall into two main areas: *embedded system design and design methodologies*[1] and *context-aware data design and management*[2]. The former is the mainstream research topic, focused on the design and analysis of **dependable computing systems**, facing the challenge of dealing with the occurrence of hard and soft device failures, due to physical defects and – more and more often – side-effects of the aggressive technology scaling we are witnessing. In these years, different architectures and technological platforms have been considered, proposing hardening methodologies and tools enabling the system to autonomously detect the occurrence of a fault and possibly mask/mitigate its effects. In the recent years, this interest has evolved towards self-adaptive systems, able to dynamically adapt to the occurrence of faults, also considering the varying conditions of the working environment. Starting with the SAVE project she is coordinating, the research interest for self-adaptive systems is taking into account heterogeneous architectures for both embedded systems and high-performance computing, investigating solutions for energy/performance trade-offs.

Context-awareness is a topic belonging to a very different area and is a research interest developed in the last ten years, when context-awareness started attracting a lot of interest, due to the increasing availability of high amount of data and pervasive/mobile systems, posing a quest for personalisation approaches. The effort in this field has been devoted to the definition of a context model and methods and tools for a **context-aware data design and access**.

More recently, Cristiana Bolchini has been involved in projects in relation to the use of ICT towards energy awareness and efficiency in smart buildings and communities. Research in this area is also progressing leading to the definition of a methodology to design and implement monitoring campaigns to collect data and exploit it for energy usage improvement and user's awareness.

In the following, the investigated issues (and related publications) are here listed, starting from the most recent, on-going activities.

Dynamic Reliability Management Methodologies for the runtime management of possibly heterogenous resources to improve fault management against transient and permanent faults as well as lifetime reliability. (publications: [IC.1][IC.2][IC.3])

Towards self-adaptive dependable systems, with dynamically tunable levels of dependability
In the past the adoption of full-fledge fault tolerance/detection techniques was an acceptable approach, because these expensive strategies were adopted only in critical application scenarios. Today, a certain level of dependability is necessary also for non-critical application environments, but having a limited budget for dependability features, therefore a tunable level of hardening must be provided, dynamically leveraging it with performance and energy. (publications: [JR.11][JR.7][IC.22][IC.18][IC.16][IC.15][IC.10])

System level reliability
By starting from a high level description of the system (e.g., in SystemC) reliability properties are analyzed and introduced during the system hardware/software co-design, targeting both classical and innovative architectures:

- design space exploration for optimal hardening (publications: [JR.10][IC.31][IC.29]);
- hardware/software co-design (publications: [JR.30][JR.20][IC.70][IC.67][IC.66] [IC.65][IC.63][IC.60][IC.59][IC.57] [IC.55][IC.46] [IC.42][IC.41][IC.40][IC.38][IC.23]);
- VLIW processor architectures (publications: [JR.26][IC.64]);

Reliable Reconfigurable platforms
Permanent and transient fault effects are mitigated by exploiting the reconfigurability available on Field Programmable Gate Arrays (FPGAs), for both single- and multi-device (publications: [JR.16][JR.14][JR.9][JR.8] [IC.62][IC.61][IC.51][IC.49] [IC.45][IC.39][IC.37][IC.35][IC.32][IC.27][IC.24] [IC.21][IC.20][IC.11])

Functional diagnosis and test
An automated, incremental functional diagnosis methodology to identify and localize faulty components in complex boards/ systems. Initially the method was based on the exploitation of an engine based on Bayes Naive Networks, most recent work is investigating the use of data mining. (publications: [JR.3][JR.5][JR.6][IC.36][IC.34][IC.33][IC.30][IC.25][IC.17] [IC.12][IC.7])

Self-adaptive heterogeneous architectures for energy/performance optimisation Solutions for the realisation of self-adaptive heterogeneous architectures optimising energy/performance trade-offs.
(publications: [IC.4][IC.5][IC.6][IC.8][IC.14][IC.13])

ICT for energy awareness in smart buildings and communities Approaches to sustainable energy usage and users' awareness.
(publications: [JR.1][JR.4][IC.9])

[1] http://hermes.ws.dei.polimi.it/
[2] http://poseidon.ws.dei.polimi.it/ca/

Previously, the attention has been devoted to the design of easily testable and self-testing digital circuits, to enable the design of dependable systems.

Design methodologies for easy-to-test digital devices
Design methodologies for applying Design-for-Testability techniques have been defined, with the aim of providing the designer a set of techniques as part of the standard design flow (publications: [JR.37][JR.35][IC.97][IC.96][IC.92][IC.94][IC.87]).

Design methodologies for designing high-quality devices
The standard design flow for the realization of digital designs has been studied and adapted to allow the verification of its various steps (from the specification) and the introduction of techniques to provide fault detection and tolerance properties. The most significant aspects taken into account are:

- device specification (publications: [IB.5][JR.33][IC.83]);
- autonomous fault detection properties (publications:[JR.34][JR.32][JR.31][JR.28][IC.89][IC.85][IC.84][IC.81][IC.78] [IC.77][IC.74][IC.72][IC.68]);
- fault tolerance properties (publications: [JR.36][IC.93][IC.95][IC.93] [IC.86][IC.80][IC.82] [IC.79] [IC.73][IC.69]);
- quality analysis (publications: [IC.75][IC.69]).

VHDL Design verification
Starting from a VHDL description, a methodology has been investigated, aiming at the formal verification of the device functionality (publications: [IC.98][IC.71]).

As far as the research area on *context-aware, data design and management*, the following lines of work have been pursued:

Embedded/portable system architectures: data management
Analysis and development of logical/physical data structures for small, embedded systems (e.g., smart cards) aimed at improving performance with respect to the technological and privacy requirements. The research – dubbed Very Small DataBases (VSDB) – led to several publications and to a prototype software light DBMS for portable devices (publications: [JR.29][JR.23][NC.3][NC.2]).

Context-aware data design, integration, customization and tailoring
A methodology and a framework (*C*ontext-*A*ware *D*ata *D*esign, *I*ntegration, *C*ustomization and *T*ailoring) for managing (selection, tailoring and integration) data from heterogeneous sources in a context-aware scenario. The research covers a broad spectrum and the specific aspects currently taken into consideration are the following ones:

- Context-ADDICT as a methodology/framework (publications: [JR.27][JR.25][JR.18][IC.56][IC.54][IC.53][IC.50] [IC.48][IC.44])
- Context modeling (publications: [JR.21] [JR.19])
- Data tailoring (publications: [JR.12][IC.47][IC.43])
- Context-awareness integrated in a broader scenario, within the ESTEEM project (publications: [JR.17][JR.15])
- Context-awareness integrated in a broader scenario, within the ART-DECO project (publications: [IB.2][IB.3])
- New perspectives (publications: [IC.26][JR.13])

Finally, it is possible to relate publications [JR.24] and [IC.58] to a collaboration starting from a graduation thesis, being further investigated, for the implementation of XCS classifier algorithms on an FPGA platform.

Collaborations

The following ones are scientific collaborations (recent ones are highlighted), besides those stemmed from joint research projects:

- University of California at Irvine (prof. N. Dutt, Dr. Amir Rahmani) on runtime resource management for heterogeneous system architetures;
- University of Piraeus (prof. M. Psarakis) on the design of a reliable/reconfigurable processor implemented on FPGAs;
- National University of Singapore (prof. A. Kumar and his PhD student Anup K. Das) on the design of dependable multicore architectures;
- National University of Singapore (prof. T. Mitra and her PhD student Thannirmalai Somu Muthukaruppan) on energy-aware dependable heterogeneous architectures;
- Brno University of Technology (prof. Z. Kotásek) on testing and functional verification (supported by MEDIAN);
- Politecnico di Torino (prof. Massimo Violante, Dr. Luca Sterpone) on the design and analysis of hardened systems implemented on FPGA platforms;
- Politecnico di Torino (prof. Maurizio Rebaudengo, prof. Massimo Violante) on the design and analysis of hardened processors by means of hw/sw techniques.

4 Current and Recent Professional Activities

National and International Research Projects

She is/has been directly responsible for the following project (on-going activities are highlighted):

- Italian National Technological Cluster 2014 - **EEB** Zero Energy Buildings in Smart Urban Districts (2014 - 20176)
  (local co-principal investigator: prof. C. Bolchini)
- European FP7 Strep Project - **SAVE** - Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures (2013 - 2016)
  (Coordinator: prof. C. Bolchini)
- European COST Action IC1103 **MEDIAN** - Manufacturable and Dependable Multicore Architectures at Nanoscale (2011 - 2015)
  (Italian MC: prof. C. Bolchini)
- Italian MIUR PRIN 2008 - High reliability fault tolerant digital systems in nanometric technologies: characterization and design methodologies (2010 - 2012)
  (local principal investigator: prof. C. Bolchini)

She contributes/contributed actively in funded research projects, more precisely (on-going activities are highlighted):

- Regione Lombardia 2014 - **SCUOLA** - Smart Campus as Urban Open LAbs (2014 - 2015)
  (local co-principal investigator: prof. A. Capone)
- European FP7 Strep Project - **FASTER** "Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration" (2011 - 2014)
  (local principal investigator: prof. D. Sciuto)
- European Artemis JU Project - **SMECY** "Smart Multicore Embedded systems" (2010 - 2013)
  (local principal investigator: prof. D. Sciuto).
- European FP7 Strep Project - **SYNAPTIC** "SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms" (2009 - 2012)
  (local principal investigator: prof. F. Ferrandi)
- European ERC Grant - **SMSCom** 'Self-Managing Situational Computing"
  (local principal investigator: prof. C. Ghezzi)
- European Artemis JU Project - **SCALOPES** "SCalable LOw Power Embedded platformS" (2009 - 2010)
  (local principal investigator: prof. D. Sciuto).
- Italian MIUR (Italian Ministry of University and Research) FIRB **ART-DECO** - Adaptive infrastructures for decentralised organizations (2006 - 2009)
  (local principal investigator: prof. L. Tanca)
- European FP6 IP Project - **hARTES** "Holistic Approach to Reconfigurable real Time Embedded Systems" (2006 - 2009)
  (local principal investigator: prof. D. Sciuto).
- Italian MIUR PRIN 2005 - **ESTEEM** - Emergent Semantics and cooperaTion in multi-knowledgE EnvironMents - Advanced methods and tools for semantic cooperation in Web virtual communities
  (local principal investigator: prof. L. Tanca)
- Italian MIUR FIRB **MAIS** - Multi-Channel Adaptive Information Systems - (2002 - 2006)
  (local principal investigator: prof. L. Tanca)
- "Design for Self-Checking multimedia systems" - CNR-Agenzia2000 (2001)
  (local principal investigator: prof. D. Sciuto)
- European Project Esprit-OMI - **REQUEST**
- European Project ESPRIT - **FORMAT** and **V-FORMAT**
- European Project ESPRIT - **PATRICIA**

Industrial/Other grants

- **Principal investigator** on Grant CG #583539 from Cisco University Research Program Fund of Silicon Valley Community Foundation for "FIND^2: A flexible functional diagnosis framework based on machine-learning techniques" - Oct. 2014/Sep. 2015, US$100.000.
- **Principal investigator** on Grant CG #574830 from Cisco University Research Program Fund of Silicon Valley Community Foundation for "Exploiting (historical) test output data to improve functional diagnosis" - Jan. 2013/Dec. 2013, US$100.000.

- **Co-Principal investigator** on Sponsored Research Agreement from Cisco Systems Inc. for "AFD (Automatic Fault Detective Analyzer)" - Jul. 2008/ Jul. 2009.
- **Co-principal advisor** on #NPI - ESA/ESTEC Contract 22079/08//NL/JK, for co-sponsored PhD on "Reliability-Aware Design Methodologies for Embedded Systems on Multi-FPGA Platforms" - Nov. 2008/Dec. 2011, €90.000 (P.I.: Donatella Sciuto, PhD: Chiara Sandionigi).
- **Principal investigator** on Grant "Young researcher funding program" from Politecnico di Milano/MURST for "Smart card reliability issues" - Sep. 2000/Aug. 2001, Lit.10.000.000.
- "Reconfigurable Computing" research within the "Electronic Design Automation" research agreement between Politecnico di Milano and Siemens Information and Communication Network SpA (1999-2000).

Conference organization

- **Chair** for the Tutorials of the European Design, Automation and Test in Europe - DATE, 2016, 2017.
- **Program Chair** for the Track T4 - System-Level Reliability Design, Analysis and On-line Test for the European Design, Automation and Test in Europe - DATE, 2017.
- **Program Co-Chair** for the Track T4 - On-Line Test, Fault Tolerance and Robust Systems for the European Design, Automation and Test in Europe - DATE, 2015, 2016.
- **Program Co-Chair** for the Friday Workshop of the European Design, Automation and Test in Europe - DATE, 2013, 2014, 2015.
- **General Co-Chair** for the 2nd MEDIAN Workshop, Avignon, F, 2013.
- **Financial Chair** for the Int. Conference on Field Programmable Logic and Applications, Milano, IT, 2010.
- **General Co-Chair** for the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems, Boston, USA, 2008.
- **Program Co-Chair** for the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems, Rome, IT, 2007.
- **General Co-Chair** for the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems, Cambridge, MA, U.S.A., 2003.
- **Program Co-Chair** for the IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems, Vancouver, Canada, 2002.

Editorial services

Dr. Bolchini has been an Associate Editors-in-Chief of the *IEEE Transactions on Emerging Topics in Computing* (2013-2015) and an Associated Editor of the *IEEE Transactions on Computers* (Sep. 2007 - Nov. 2012) and a Guest Editor for the same journal, for Springer Journal of Electronic Testing: Theory and Applications, for Elsevier Journal of Systems Architectures, and for Elsevier Microprocessors and Microsystems: Embedded Hardware Design for special sessions on Dependability-related special issues. She has been a Guest Editor for a Special Sessions on *IEEE Trans. on Computers*, and a Joint Special Section on *IEEE Trans. on Computers* and *IEEE Trans. on Nanotechnology* on Defect and Fault Tolerance in VLSI and Nanotechnology Systems.

Membership

Cristiana Bolchini is an IEEE Senior Member (2009), an IEEE Computer Society Member (1995), and a HiPEAC Member (2012).

Technical Program Committee Membership

Dr. Bolchini participates to program committees of conference and symposium focusing on fault tolerance and reliability issues, more precisely:

- IEEE/ACM Int. Conf. on Computer-Aided Design – ICCAD (2014)
- ACM/EDAC/IEEE Design Automation Conference – DAC (2012-2013)
- IEEE/ACM Design, Automation and Test in Europe Conference – DATE, "On-Line Testing, Fault Tolerance, and Reliability" Track (2004-2009, 2012-present)
- IEEE Int. Conference on on Computer Design – ICCD (2013-present)
- IEEE Int. Symposium on Defect and Fault Tolerance in VLSI Systems – DFT (2001-present)
- IEEE International On-Line Testing Symposium (former International On-Line Testing Workshop) – IOLTS (2002-2009, 2012-2014)
- IEEE International On-Line Testing Symposium (former International On-Line Testing Workshop) – IOLTS (2002-2009, 2012-2014)

- Euromicro Conference on Digital System Design, Architectures, Methods and Tools, Special Session on "Dependability, Testing and Fault-Tolerance in Digital Systems" – DSD (2014-)
- Euromicro Conference on Digital System Design, Architectures, Methods and Tools, Special Session on "Fault Tolerance in Digital System Design" – DSD (2008-2014)
- Int. Conference on Field Programmable Logic and Applications – FPL (2010-present)
- NASA/ESA Conference on Adaptive Hardware and Systems (2013-2014)
- HiPEAC Workshop on Design for Reliability (2010-2013)
- HiPEAC Workshop on Reconfigurable Computing (2013-2016)
- Southern Programmable Logic Conference (2012, 2014)

Referee services

Dr. Bolchini is a referee for the following journals *IEEE Transactions on Computers*, *IEEE Transactions on VLSI Systems*, *IEEE Transactions on Instrumentation and Measurements*, *IEEE Transactions on Reliability*, *Elsevier Journal of System Architectures*, *Springer Journal of Electronic Testing*, *IEEE Design & Test of Computers*, *ACM Transactions on Design Automation of Electronic Systems*, *ACM Transactions on Embedded Computing Systems IEEE Transactions on Nanotechnology* and the *ACM Communications Computing Reviews*.

Furthermore, she reviews papers submitted to conferences, workshops and symposia (*IEEE Design Automation Conference*, *IEEE/ACM Int. Conf. on Computer-Aided Design*, *IEEE Design, Automation and Test in Europe*, *IEEE International Test Conference*, *IEEE Defect and Fault Tolerance in VLSI Systems*, *IEEE On-Line Testing Symposium*, *IEEE European Test Symposium*, *IEEE VLSI Test Symposium*, *IEEE Great Lake Symposium on VLSI*, *Southern Programmable Logic Conference*).

5 Teaching activity

Since the academic year 1997/98 Cristiana Bolchini has been lecturing, at first as an assistant, later as the course lecturer (before holding an Assistant/Associate Professor position), at Politecnico di Milano (various campuses) and at Libero Istituto Carlo Cattaneo. She has been teaching the introductory course to Fundamentals of Computer Science to freshmen for more than fifteen years (undergraduate course with 160+ students) engaging students from different engineering tracks (Computer Science Engineering in the last years, Mechanical Engineering earlier) in problem solving and C programming, receiving very positive evaluations from the students. Moreover, she taught the Digital Logic Design course to undergraduate Computer Science Engineering students. In the last years she is teaching also a graduate course on Dependable Systems, introducing a methodological approach to system dependability by introducing the basic concepts in terms of dependability attributes, fault/failure models, methods to design and analyze this class of systems, also presenting practical solutions for their realization.

Academic courses

Year	Course	Faculty	U/G/Phd
Professor			
2016-2017	Dependable Systems	Computer Science Engineering	G
2015-2016	Fundamentals of Computer Science	Computer Science Engineering	U
Associate Professor			
2014-2015			
2013-2014	Dependable Systems	Computer Science Engineering	G
2012-2013	Digital Logic Design	Computer Science Engineering	U
2011-2012	Fundamentals of Computer Science	Computer Science Engineering	U
2010-2011	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U
2009-2010	Dependable Computing Systems	Computer Science Engineering	G
	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U
2008-2009	Data management for context-aware, mobile systems	Information Technology PhD	PhD
	Reliable Pervasive Computing Systems	Information Technology PhD	PhD
	Dependable Computing Systems	Computer Science Engineering	G
	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U

2007-2008	Operating Systems	Computer Science Engineering	G
	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U
2006-2007	Data management for context-aware, mobile systems	Information Technology PhD	PhD
	Reliable Pervasive Computing Systems	Information Technology PhD	PhD
	Operating Systems	Computer Science Engineering	G
	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U
2005-2006	Dependable Computing Systems	Computer Science Engineering	G
	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U
	Fundamentals of Computer Science	Mechanical Engineering	U
2004-2005	Digital Logic Design	Computer Science Engineering	U
	Fundamentals of Computer Science	Computer Science Engineering	U
	Fundamentals of Computer Science	Mechanical Engineering	U
2003-2004	Fundamentals of Computer Science	Computer Science Engineering	U
	Fundamentals of Computer Science	Mechanical Engineering	U
Assistant Professor			
2002-2003	Fundamentals of Computer Science	Computer Science Engineering	U
	Fundamentals of Computer Science	Mechanical Engineering	U
2001-2002	Fundamentals of Computer Science	Aeronautical Engineering	U
	Fundamentals of Computer Science	Mechanical Engineering	U
2000-2001	Fundamentals of Computer Science	Mechanical Engineering	U
	Computing Systems	Electronics, Automation, Telecommunication and Computer Science Engineering	D
1999-2000	Fundamentals of Computer Science	Management Engineering	U
	Fundamentals of Computer Science	Environmental Engineering	U
Contracts			
1998-1999	Computer Graphics	Building Engineering *Politecnico di Milano*	U
	Fundamentals of Computer Science	Business Administration and Management *Libero Istituto Carlo Cattaneo*	U
1997-1998	Fundamentals of Computer Science	Environmental Engineering *Politecnico di Milano*	U
	Fundamentals of Computer Science	Business Administration and Management *Libero Istituto Carlo Cattaneo*	U

U: undergraduate level, G: graduate level, PhD: phd level, D: Diploma Universitario

Professional courses

Teaching activity for scientific training for companies (Alcatel, TXT, Italtel, Siemens,...) on:
- VHDL language,
- Digital design with VHDL,
- Computer architectures,
- C Language.

Students' supervision

Since 1993 Cristiana Bolchini has supervised students for their graduation thesis projects, either as an advisor or co-advisor, on research related to digital design, reliable design and the context-aware data design and management. Often such studies have led to scientific publications. A list of recent student supervision is reported in the following.

PhD Students Supervision

Angela Geronazzo 2014-, Topic: Energy Efficiency in Buildings: A data perspective
Matteo Carminati 2012-2014, "Towards the Definition of a Methodology for the Design of Tunable Dependable Systems"
Chiara Sandionigi 2009-2011, "A reliability-aware design methodology for embedded systems on multi-FPGA platforms"
Antonio Miele 2007-2009, "A methodology for the design and analysis of reliable embedded systems"
Francesco Merlo Minor Research Supervision, "A graph-based framework for querying and modeling integrated sources"
Barbara Oliboni Minor Research Supervision, "Data access policies for very small databases"

Research Assistants Supervision

Giovanni Bettinazzi 2014-2015, "Energy monitoring and awareness in Smart Campus as Urban Open Labs",
Luca Cassano 2014-2015, "FIND^2: A flexible functional diagnosis framework based on machine learning techniques",
Luca Cassano 2013-2014, "Statistical and machine-learning based techniques for the functional diagnosis of complex systems",
Mohammad Ali Tabibi 2013, "Definition and development of a software tool for the automatic diagnosis of faults in complex systems, based on data mined rules"

PhD Students Committees

Xinhai Zhang 2017, "Automated Support for the Architecting of Distributed Embedded Systems: Method and Analysis for Industrial Adoption", PhD program in Computer Engineering of KTH, Computer Science and Engineering Department – Member of the dissertation committee for the PhD defense.
Stavros Tzilis 2015, "Runtime system management of gracefully degradable adaptive SoCs", PhD program in Computer Engineering of the Chalmers University of Technology, Computer Science and Engineering Department – PhD Licentiate Discussion Leader
Luigi Di Guglielmo 2012, "Realizability of embedded controllers: from hybrid models to correct implementations", PhD program in Computer Science of the University of Verona, Department of Computer Science – Defence Jury Member

Graduate Students Supervision

Stefano Bielli -, Topic: Runtime Resource Management for Dependability-Aware Multicore Systems
Renzo Cancho -, "Dependability analysis and design methods for FPUs"
Stefano Guidobaldi 2011, "Enhanced Software Error Analysis Methodology"
Fabrizio Castro 2009, "Design and implementation of a tool for fault injection in SRAM-based FPGAs"

Foreign students supervision

Clara Casas Castedo 2013, Master Thesis, "Reliable system design for Zynq platforms" (Universidad Politécnica de Madrid)
Miguel Baquero Gago 2013, Master Thesis, "Performance-aware system design for Zynq platforms" (Universidad Politécnica de Madrid)
Anup K. Das May-July 2013, PhD candidate, "Dependable adaptable multi-core systems" (National University of Singapore)
Naser Derakhshan 2012, "Dependable Configuration Controller for Multi-FPGA Platforms" (Royal Institute of Technology – KTH)
Marcela Šimková June 2012, "Testing of qualities of fault-tolerant methodologies to increase the reliability of digital systems " (Brno University of Technology)
Jan Kaštil June 2012, "Testing of qualities of fault-tolerant methodologies to increase the reliability of digital systems " (Brno University of Technology)
Francisco Tejero Calvo 2010, "A methodology for the design of SRAM-based FPGAs able to tolerate permanent faults" (Universidad de Sevilla).

6 Academic services/responsibilities

During the years at Politecnico di Milano the following services/roles for the institution have been held:

- member of the Computer Science section board (2013-present)
- vice-head of the PhD board in Information Technology for the Computer Science section (2016-present)
- member of the Committee for Abilitazione Scientifica Nazionale - SC 09/H1 - Sistemi per l'elaborazione (2016-present)
- Rector's delegate (with prof. Marco Imperadori) for International Relationships with the Far East (2017/2019)
- member of the committee for courses scheduling (2002-2013)
- member of the PhD Final Examination Committee (2011)
- member of the Technical Committee evaluating the opportunity to file for a patent (2008)
- member of the PhD Admission Committee (2007)
- member of the department committee for the web for the Computer Science Engineering area (2003-2006)

- member of the department board (2003-2004)
- adjunct member for the Evaluation Committee of State Exams for the Qualification to the Engineering Profession (2003-2004)

7 Selected publications

These are the top ten selected publications, according to Cristiana Bolchini.

1. C. Bolchini, L. Cassano, "A Novel Approach to Incremental Functional Diagnosis for Complex Electronic Boards" *IEEE Trans. on Computers*, Vol. 65, No. 1, (2016), pp. 42-52, (ISSN: 0018-9340) – Rif. [JR.5]
   [doi: http://dx.doi.org/10.1109/TC.2015.2417537]
2. C. Bolchini, L. Cassano, P. Garza, E. Quintarelli, F. Salice, "An Expert CAD Flow for Incremental Functional Diagnosis of Complex Electronic Boards" *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, in press, (ISSN: 0278-0070) – Rif. [JR.6]
   [doi: http://dx.doi.org/10.1109/TCAD.2015.2396997]
3. C. Bolchini, C. Sandionigi, "Design of Hardened Embedded Systems on Multi-FPGA Platforms" *ACM Trans. on Design Automation of Electronic Systems*, Vol. 20, No. 1, (2014), pp. 16:1-16:26, (ISSN: 1084-4309) – Rif. [JR.8]
   [doi: http://dx.doi.org/10.1145/2676551]
4. C. Bolchini, A. Miele, "Reliability-driven System-level Synthesis for Mixed-Critical Embedded Systems" *IEEE Trans. on Computers,* Vol. 62, no. 12 (2013), pp. 2489-2502, (ISSN: 0018-9340) – Rif. [JR.10]
   [doi: http://dx.doi.org/10.1109/TC.2012.226]
5. C. Bolchini, E. Quintarelli, L. Tanca, "CARVE: Context-aware automatic view definition over relational databases" *Information Systems, Elsevier* Vol. 38, no. 1, (2013), pp. 45-67, (ISSN: 0306-4379) – Rif. [JR.12]
   [doi: http://dx.doi.org/10.1016/j.is.2012.05.004]
6. C. Bolchini, A. Miele, C. Sandionigi, "A Novel Design Methodology for Implementing Reliability-Aware Systems on SRAM-Based FPGAs," *IEEE Trans. on Computers,* Vol. 60, No. 12, (2011), pp. 1744-1758, (ISSN: 0018-9340) – Rif. [JR.14]
   [doi: http://dx.doi.org/10.1109/TC.2010.281]
7. D. Bianchini, S. Montanelli, C. Aiello, R. Baldoni, C. Bolchini, S. Bonomi, S. Castano, T. Catarci, V. De Antonellis, A. Ferrara, M. Melchiori, E. Quintarelli, M. Scannapieco, F. A. Schreiber, L. Tanca, "Emergent Semantics and Cooperation in Multi-knowledge Communities: the ESTEEM Approach," *World Wide Web, Springer* Vol. 13, no. 1-2, (2010), pp. 3-31 (ISSN: 1386-145X) – Rif. [JR.17]
   [doi: http://dx.doi.org/10.1007/s11280-009-0080-6]
8. C. Bolchini, C. A. Curino, E. Quintarelli, F. A. Schreiber, L. Tanca, "A Data-oriented Survey of Context Models," *ACM SIGMOD Record,* Vol. 36, no 4, (2007), pp. 19–26. (ISSN:0163-5808) – Rif. [JR.21]
   [doi: http://doi.acm.org/10.1145/1361348.1361353]
9. C. Bolchini, F. A. Schreiber, L. Tanca, "A methodology for a Very Small Data Base design," *Information Systems, Elsevier,* Vol. 32, no. 1, (2007), pp. 61–82. (ISSN:0306-4379) – Rif. [JR.23]
   [doi: http://dx.doi.org/10.1016/j.is.2005.05.004]
10. C. Bolchini, "A Software Methodology for Detecting Hardware Faults in VLIW Data Paths," *IEEE Trans. on Reliability,* (TR) Vol. 52, no. 4, (2003), pp. 458–468. (ISSN: 0018-9529/03) – Rif. [JR.26]
    [doi: http://dx.doi.org/10.1109/TR.2003.821935]

8 Complete publication list

Publication list [3]

Refereed international journals	36
Editorial contributions	9
Refereed international books and book chapters	4
National scientific books and book chapters	1
Refereed international conferences	99
Refereed national conferences	3
Refereed international workshops	1

[3] In Italy, authors typically appear in alphabetical order

Refereed international journals

JR.1. with A. Geronazzo and E. Quintarelli, "Smart buildings: a monitoring and data analysis methodological framework" *Elsevier Building and Environment*, Vol. 121, (2017), pp. 93-105, (ISSN: 0360-1323)
[doi: http://dx.doi.org/10.1016/j.buildenv.2017.05.014]
[Scopus:2-s2.0-85019473001]

JR.2. with M.-H. Haghbayan, A. Miele, A. M. Rahmani, P. Liljeberg, A. Jantsch, and H. Tenhunen "Can Dark Silicon Be Exploited to Prolong System Lifetime?" *IEEE Design & Test*, Vol. 34, No. 2, (2017), pp. 51-59, (ISSN: 2168-2356)
[doi: http://dx.doi.org/10.1109/MDAT.2016.2630317]
[Scopus:2-s2.0-85014721125]

JR.3. with L. Cassano, "A Fully Automated and Configurable Cost-Aware Framework for Adaptive Functional Diagnosis" *IEEE Design & Test*,Vol. 34, No. 2, (2017), pp. 79-86, (ISSN: 2168-2356)
[doi: http://dx.doi.org/10.1109/MDAT.2016.2550584]
[Scopus:2-s2.0-85014682023]

JR.4. with A. Barbato, A. Geronazzo, E. Quintarelli, A. Palamarciuc, A. Pitì, C. Rottondi, G. Verticale, "Energy Optimization and Management of Demand Response Interactions in a Smart Campus" *Energies, MDPI*, Vol. 9, no. 6, (2016), pp. 398-417 (EISSN 1996-1073)
[doi: http://dx.doi.org/10.3390/en9060398]
[Scopus:2-s2.0-84996508802] [WOS:000378854400011]

JR.5. with L. Cassano, "A Novel Approach to Incremental Functional Diagnosis for Complex Electronic Boards" *IEEE Trans. on Computers*, Vol. 65, no. 1, (2016), pp. 42-52, (ISSN: 0018-9340)
[doi: http://dx.doi.org/10.1109/TC.2015.2417537]
[Scopus:2-s2.0-84961728578] [WOS:000366419400005]

JR.6. with L. Cassano, P. Garza, E. Quintarelli, F. Salice, "An Expert CAD Flow for Incremental Functional Diagnosis of Complex Electronic Boards" *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, Vol. 34, no. 5, (2015), pp. 835-848, (ISSN: 0278-0070)
[doi: http://dx.doi.org/10.1109/TCAD.2015.2396997]
[Scopus:2-s2.0-84928381405]

JR.7. M. Ottavi, S. Pontarelli, D. Gizopoulos, C. Bolchini, M. K. Michael, L. Anghel, M. Tahoori, A. Paschalis, P. Reviriego, O. Bringmann, V. Izosimov, H. Manhaeve, C. Strydis, S. Hamdioui, "Dependable Multicore Architectures at Nanoscale and their Applications: the view from Europe" *IEEE Design & Test*, Vol. 32, no. 2, (2015), pp. 17-28, (ISSN: 2168-2356)
[doi: http://dx.doi.org/10.1109/MDAT.2014.2359572]
[Scopus:2-s2.0-84926315110] [WOS:000354407400003]

JR.8. with C. Sandionigi, "Design of Hardened Embedded Systems on Multi-FPGA Platforms" *ACM Trans. on Design Automation of Electronic Systems*, Vol. 20, no. 1, (2014), pp. 16:1–16:26, (ISSN: 1084-4309)
[doi: http://dx.doi.org/10.1145/2676551]
[Scopus:2-s2.0-84914674733]

JR.9. with A. Miele, C. Sandionigi, "Autonomous fault-tolerant systems onto SRAM-based FPGA platforms" *Journal of Electronic Testing - Theory and Applications, Springer*, Vol. 29, no. 6, (2013), pp. 779-793, (ISSN: 0923-8174)
[doi: http://dx.doi.org/10.1007/s10836-013-5418-4]
[Scopus:2-s2.0-84891631927]

JR.10. with A. Miele, "Reliability-driven System-level Synthesis for Mixed-Critical Embedded Systems" *IEEE Trans. on Computers,* Vol. 62, no. 12 (2013), pp. 2489-2502, (ISSN: 0018-9340)
[doi: http://dx.doi.org/10.1109/TC.2012.226]
[Scopus:2-s2.0-84888121879]

JR.11. with M. Carminati, A. Miele, "Self-Adaptive Fault Tolerance in Multi-/Many-Core Systems" *Journal of Electronic Testing - Theory and Applications, Springer,* Vol. 29, no. 2, (2013), pp. 159-175, (ISSN: 0923-8174)
[doi: http://dx.doi.org/10.1007/s10836-013-5367-y]
[Scopus:2-s2.0-84877799632]

JR.12. with E. Quintarelli, L. Tanca, "CARVE: Context-aware automatic view definition over relational databases" *Information Systems, Elsevier,* Vol. 38, no. 1, (2013), pp. 45-67, (ISSN: 0306-4379)
[doi: http://dx.doi.org/10.1016/j.is.2012.05.004]
[Scopus:2-s2.0-84869218859]

JR.13. with G. Orsi, E. Quintarelli, F. A. Schreiber, L. Tanca, "Context Modeling and Context Awareness: steps forward in the Context-ADDICT project," *IEEE Data Eng. Bull.* Vol. 34, no. 2, (2011), pp. 47-54

JR.14. with A. Miele, C. Sandionigi, "A Novel Design Methodology for Implementing Reliability-Aware Systems on SRAM-Based FPGAs," *IEEE Trans. on Computers,* Vol. 60, No. 12, (2011), pp. 1744-1758, (ISSN: 0018-9340)
[doi: http://dx.doi.org/10.1109/TC.2010.281]
[Scopus:2-s2.0-84864672059]

JR.15. with S. Montanelli D. Bianchini, C. Aiello, R. Baldoni, S. Bonomi, S. Castano, T. Catarci, V. De Antonellis, A. Ferrara, M. Melchiori, E. Quintarelli, M. Scannapieco, F. A. Schreiber, L. Tanca, "The ESTEEM platform: enabling P2P semantic collaboration through emerging collective knowledge," *Journal of Intelligent Information Systems, Springer,* Vol. 36, no. 2, (2011), pp. 167-195 (ISSN: 0925-9902)
[doi: http://dx.doi.org/10.1007/s10844-010-0125-4]
[Scopus:2-s2.0-79952184403]

JR.16. with C. Sandionigi, "Fault Classification for SRAM-Based FPGAs in the Space Environment for Fault Mitigation," *IEEE Embedded Systems Letters,* Vol. 2, no. 4, (2010), pp. 107-110 (ISSN: 1943-0663)
[doi: http://dx.doi.org/10.1109/LES.2010.2073441]
[Scopus:2-s2.0-78650644639]

JR.17. with D. Bianchini, S. Montanelli, C. Aiello, R. Baldoni, S. Bonomi, S. Castano, T. Catarci, V. De Antonellis, A. Ferrara, M. Melchiori, E. Quintarelli, M. Scannapieco, F. A. Schreiber, L. Tanca, "Emergent Semantics and Cooperation in Multi-knowledge Communities: the ESTEEM Approach," *World Wide Web, Springer,* Vol. 13, no. 1-2, (2010), pp. 3-31 (ISSN: 1386-145X)
[doi: http://dx.doi.org/10.1007/s11280-009-0080-6]
[Scopus:2-s2.0-77954433138]

JR.18. with C. A. Curino, G. Orsi, E. Quintarelli, R. Rossato, F. A. Schreiber, L. Tanca, "And what can context do for data?," *Communications of the ACM,* Vol. 52, no. 11, (2009), pp. 136–140. (ISSN: 0001-0782)
[doi: http://doi.acm.org/10.1145/1592761.1592793]
[Scopus:2-s2.0-70350759690]

JR.19. with C. A. Curino, E. Quintarelli, F. A. Schreiber, L. Tanca, "Context Information for Knowledge Reshaping," *Int. J. of Web Engineering and Technology,* Special Issue on Web-based Knowledge Representation and Management, Vol. 5, no. 1, (2009), pp. 88–103. (ISSN: 1476-1289)
[doi: http://dx.doi.org/10.1504/IJWET.2009.025015]
[Scopus:2-s2.0-67649199574]

JR.20. with A. Miele, M. Rebaudengo, F. Salice, D. Sciuto, L. Sterpone, M. Violante, "Software and Hardware Techniques for SEU Detection in IP Processors," *Journal of Electronic Testing: Theory and Applications, Springer,* Vol. 24, no. 1-3, (2008), pp. 35–44. (ISSN: 0923-8174)
[doi: http://dx.doi.org/10.1007/s10836-007-5028-0]
[Scopus:2-s2.0-40949123750]

JR.21. with C. A. Curino, E. Quintarelli, F. A. Schreiber, L. Tanca, "A Data-oriented Survey of Context Models," *ACM SIGMOD Record,* Vol. 36, no 4, (2007), pp. 19–26. (ISSN:0163-5808)
[doi: http://doi.acm.org/10.1145/1361348.1361353]
[Scopus:2-s2.0-41849120869]

JR.22. with S. Ceri, D. Braga, M. Brambilla, A. Campi, S. Comai, P. Fraternali, P. L. Lanzi, M. Masseroli, M. Matera, M. Negri, G. Pelagatti, G. Pozzi, E. Quintarelli, F. A. Schreiber, L. Tanca, "Data and web management research at Politecnico di Milano," *ACM SIGMOD Record,* Vol. 36, no 4, (2007), pp. 43–48 (ISSN:0163-5808)
[doi: http://doi.acm.org/10.1145/1361348.1361359]
[Scopus:2-s2.0-41849108837]

JR.23. with F. A. Schreiber, L. Tanca, "A methodology for a Very Small Data Base design," *Information Systems, Elsevier,* Vol. 32, no. 1, (2007), pp. 61–82. (ISSN:0306-4379).
[doi: http://dx.doi.org/10.1016/j.is.2005.05.004]
[Scopus:2-s2.0-33749569281]

JR.24. with P. Ferrandi, P. L. Lanzi, F. Salice, "Evolving Classifiers on Field Programmable Gate Arrays: Migrating XCS to FPGAs," *Journal of System Architecture, Special issue on Nature Inspired Applied Systems, Elsevier* Vol. 52, no. 8-9, (2006), pp. 516–533 (ISSN:1383-7621).
[doi: http://dx.doi.org/10.1016/j.sysarc.2006.02.007]
[Scopus:2-s2.0-33745871651]

JR.25. with F. A. Schreiber, L. Tanca, "A context-aware methodology for very small data base design," *ACM SIGMOD Record,* Vol. 33, no 1, (2004), pp. 71–76. (ISSN:0163-5808)
[doi: http://doi.acm.org/10.1145/974121.974134]
doi: http://www.scopus.com/inward/record.url?eid=2-s2.0-14344266209&partnerID=40&md5=aa57c6ca9c0efaf13fbb4f5de45c
s2.0-14344266209]

JR.26. "A Software Methodology for Detecting Hardware Faults in VLIW Data Paths," *IEEE Trans. on Reliability,* (TR) Vol. 52, no. 4, (2003), pp. 458–468. (ISSN: 0018-9529/03)
[doi: http://dx.doi.org/10.1109/TR.2003.821935]
[Scopus:2-s2.0-0742324995]

JR.27. with F. Salice, F. A. Schreiber, L. Tanca, "Logical and Physical Design Issues for Smart Card Databases," *ACM Trans. on Information Systems,* (TOIS), Vol. 21, no. 3, (2003), pp. 254–285. (ISSN: 1046-8188)
[doi: http://doi.acm.org/10.1145/858476.858478]
[Scopus:2-s2.0-2442517723]

JR.28. with L. Pomante, F. Salice, D. Sciuto, "The Design of Reliable Devices for Mission Critical Applications," *IEEE Trans. on Instrumentation and Measurement,* (TIM) Vol. 52, no. 6, (2003), pp. 1703–1712. (ISSN: 0018-9456/03)
[doi: http://dx.doi.org/10.1109/TIM.2003.818736]
[Scopus:2-s2.0-0344013030]

JR.29. with F. A. Schreiber, "Smart Card Embedded Information Systems: a Methodology for Privacy Oriented Architectural Design," *Data & Knowledge Engineering, Elsevier Science, Amsterdam,* Vol. 41, no. 2-3, (2002), pp. 159–182. (ISSN: 0169-023X)
[doi: http://dx.doi.org/10.1016/S0169-023X(02)00039-3]
[Scopus:2-s2.0-6444244870]

JR.30. with L. Pomante, F. Salice, D. Sciuto, "Reliability Properties Assessment at System Level: A Co-design framework," *Journal of Electronic Testing - Theory and Application, Kluwer Academic Publishers,* Vol. 18, no. 3, (2002), pp. 351–356. (ISSN 0923-8174)
[doi: http://dx.doi.org/10.1023/A:1015047524985]
[Scopus:2-s2.0-0036605168]

JR.31. with R. Montandon, F. Salice, D. Sciuto, "Design of VHDL Based Totally self-checking Finite State Machine and Data Path Descriptions," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems, (TVLSI)* Vol. 8, no. 1, (2000), pp. 82-102. (ISSN: 1063-8210)
[doi: http://dx.doi.org/10.1109/92.820766]
[Scopus:2-s2.0-0034135608]

JR.32. with F. Salice, D. Sciuto, "Fault Analysis for Networks with Concurrent Error Detection Properties," *IEEE Design and Test of Computers,* Vol. 15, no. 4, (1998), pp. 66-74. (ISSN: 0740-7475)
[doi: http://dx.doi.org/10.1109/54.735929]
[Scopus:2-s2.0-0032181144]

JR.33. with L. Baresi, "Software Methodologies for VHDL Code Static Analysis," *Journal of Systems Architecture, Elsevier Science, North Holland,* Vol. 44, n. 1, (1997), pp. 3-21. (ISSN: 1383-7621/0165-6074)
[doi: http://dx.doi.org/10.1016/S1383-7621(97)00024-6]
[Scopus:2-s2.0-0031256195]

JR.34. with F. Salice, D. Sciuto "Design of Totally Self Checking Checkers for a Class of Constant Hamming Distance Codes," *Journal of Microelectronic Systems Integration, Plenum Press, New York,* Vol. 5, no. 2, (1997), pp. 85–100. (ISSN: 1070-0056)

JR.35. with M. Bombana, G. Buonanno, P. Cavalloro, F. Ferrandi, D. Sciuto, "A Wafer Level Testability Approach Based on an Improved Scan Insertion Technique," *IEEE Trans. on Components, Packaging and Manufacturing Technology B,* (TCPMT-B), Vol. 18, no. 3, (1995), pp. 438–447. (ISSN: 1070-9894)
[doi: http://dx.doi.org/10.1109/96.404100]
[Scopus:2-s2.0-0029359219]

JR.36. with G. Buonanno, D. Sciuto, R. Stefanelli, "CMOS Fault Tolerant Architectures for Switch Level Faults," *Journal of Microelectronic Systems Integration, Plenum Press, New York,* (JMSI), Vol. 3, no. 2, (1995), pp. 121–139. (ISSN: 1070-0056)

JR.37. with F. Fummi, D. Sciuto, "Two-Dimensional Sequential Arrays: Design For Testability and Reconfiguration Issues," *Journal of Microelectronic Systems Integration, Plenum Press, New York,* (JMSI), Vol. 1, no. 3/4, (1993), pp. 209–220. (ISSN: 1070-0056)

Editorial contributions

ED.1. C. Bolchini, S. Kundu and S. Pontarelli, "Guest Editorial IEEE Transactions on Computers and IEEE Transactions on Nanotechnology Joint Special Section on Defect and Fault Tolerance in VLSI and Nanotechnology Systems," *IEEE Trans. on Computers, IEEE Trans. on Nanotechnology*, Vol. 65, no. 3, pp. 677-678, 2016.
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