Preface

Image sensors have recently attracted renewed interest for use in digital cameras, mobile phone cameras, handy camcorders, cameras in automobiles, and other devices. For these applications, CMOS image sensors are widely used because they feature on-chip integration of the signal processing circuitry. CMOS image sensors for such specific purposes are sometimes called smart CMOS image sensors, vision chips, computational image sensors, etc.

Smart CMOS Image Sensors & Applications focuses on smart functions implemented in CMOS image sensors and their applications. Some sensors have already been commercialized, whereas some have only been proposed; the field of smart CMOS image sensors is active and generating new types of sensors. In this book I have endeavored to gather references related to smart CMOS image sensors and their applications; however, the field is so vast that it is likely that some topics are not described. Furthermore, the progress in the field is so rapid that some topics will develop as the book is being written. However, I believe the essentials of smart CMOS image sensors are sufficiently covered and that this book is therefore useful for graduate school students and engineers entering the field.

This book is organized as follows. First, MOS imagers and smart CMOS image sensors are introduced. The second chapter then describes the fundamental elements of CMOS image sensors and details the relevant optoelectronic device physics. Typical CMOS image sensor structures, such as the active pixel sensor (APS), are introduced in this chapter. The subsequent chapters form the main part of the book, namely a description of smart imagers. Chapter 3 introduces several functions for smart CMOS image sensors. Using these functions, Chapter 4 describes smart imaging, such as wide dynamic range image sensing, target tracking, and three-dimensional range finding. In the final chapter, Chapter 5, several examples of applications of smart CMOS image sensors are described.

This work is inspired by numerous preceding books related to CMOS image sensors. In particular, A. Moini’s, “Vision Chips” [1], which features a comprehensive archive of vision chips, J. Nakamura’s, “Image Sensors and Signal Processing for Digital Still Cameras” [2], which presents recent rich results of this field, K. Yonemoto’s introductory but comprehensive book on CCD and CMOS imagers, “Fundamentals and Applications of CCD/CMOS Image Sensors” [3] and O. Yadid-Pecht and R. Etienne-Cummings’s book, “CMOS Imagers: From Phototransduction To Image Processing” [4]. Of these, I was particularly impressed by K. Yonemoto’s book, which unfortunately has only been published in Japanese. I hope that the present work helps to illuminate this field and that it complements that of Yonemoto’s book.
I have also been influenced by books written by numerous other senior Japanese researchers in this field, including Y. Takamura [5], Y. Kiuchi [6] and T. Ando and H. Komobuchi [7]. The book on CCDs by A.J.P. Theuwissen is also useful [8].

I would like to thank the many people who have contributed both directly and indirectly to the areas covered in this book. Particularly, the colleagues in my laboratory, the Laboratory of Photonic Device Science in the Graduate School of Materials Science at the Nara Institute of Science and Technology (NAIST), Prof. Takashi Tokuda and Prof. Keiichiro Kagawa have made meaningful and significant contributions, which form the main parts of Chapter 5. This book would not have been born without their efforts. Prof. Masahiro Nunoshita for his continuous encouragement in the early stages of our laboratory. Kazumi Matsumoto, the secretary of our laboratory, for her constant support in numerous administrative affairs. Finally, the graduate students of my laboratory, both past and present, are thanked for their fruitful research. I would like to extend my most sincere thanks to all of these people.

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I first entered the research area of smart CMOS image sensors as a visiting researcher at University of Colorado at Boulder under Prof. Kristina M. Johnson in 1992 to 1993. My experience there was very exciting and it helped me enormously in my initial research into smart CMOS image sensors after returning to Mitsubishi Electric Corporation. I would like to thank all of my colleagues at Mitsubishi Electric Corp. for their help and support, including Prof. Hiforumi Kimata, Dr. Shuichii Tai, Dr. Kazumasa Mitsunaga, Prof. Yutaka Arima, Prof. Masahiro Takahashi, Masaya Oita, Dr. Yoshikazu Nitta, Dr. Eiichi Funatsu, Dr. Kazunari Miyake, Takashi Toyo da, and numerous others.

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Jun Ohta,
Nara, July 2007
About the author

Jun Ohta was born in Gifu, Japan in 1958. He received his B.E., M.E., and Dr. Eng. degrees in applied physics, all from the University of Tokyo, Japan, in 1981, 1983, and 1992, respectively. In 1983, he joined Mitsubishi Electric Corporation, Hyogo, Japan, where he has been engaged in the research on optoelectronic integrated circuits, optical neural networks, and artificial retina chips. From 1992 to 1993, he was a visiting researcher in Optoelectronic Computing Systems Center, University of Colorado in Boulder. In 1998, he became an Associate Professor at the Graduate School of Materials Science, Nara Institute of Science and Technology (NAIST), in Nara, Japan, and in 2004, he became a Professor of NAIST. His current research interests include vision chips, CMOS image sensors, retinal prosthesis devices, bio-photonic LSIs, integrated photonic devices. Dr. Ohta received the Best Paper Award of the IEICE Japan in 1992, the Ichimura Award in 1996, the National Commendation for Invention in 2001, and the Niwa Takayanagi Award in 2007. He is a member of the Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Image Information and Television Engineers of Japan, Japanese Society for Medical and Biological Engineering, the Institute of Electronic and Electronics Engineers, and the Optical Society of America.
# Contents

1 Introduction ........................................ 1
   1.1 A general overview .............................. 1
   1.2 Brief history of CMOS image sensors .......... 2
   1.3 Brief history of smart CMOS image sensors ... 5
   1.4 Organization of the book ........................ 8

2 Fundamentals of CMOS image sensors .............. 11
   2.1 Introduction .................................. 11
   2.2 Fundamentals of photodetection ................. 12
      2.2.1 Absorption coefficient .................... 12
      2.2.2 Behavior of minority carriers ............. 13
      2.2.3 Sensitivity and quantum efficiency ......... 15
   2.3 Photodetectors for smart CMOS image sensors ... 17
      2.3.1 pn-junction photodiode ..................... 18
      2.3.2 Photogate .................................. 26
      2.3.3 Phototransistor ............................. 26
      2.3.4 Avalanche photodiode ....................... 27
      2.3.5 Photoconductive detector ................... 27
   2.4 Accumulation mode in PDs ....................... 29
      2.4.1 Potential change in accumulation mode ....... 30
      2.4.2 Potential description ....................... 30
      2.4.3 Behavior of photo-generated carriers in PD ... 32
   2.5 Basic pixel structures .......................... 36
      2.5.1 Passive pixel sensor ......................... 36
      2.5.2 Active pixel sensor, 3T-APS ................. 38
      2.5.3 Active pixel sensor, 4T-APS ................. 40
   2.6 Sensor peripherals .............................. 42
      2.6.1 Addressing .................................. 42
      2.6.2 Readout circuits ............................ 45
      2.6.3 Analog-to-digital converters ................. 46
   2.7 Basic sensor characteristics ...................... 48
      2.7.1 Noise ....................................... 48
      2.7.2 Dynamic range ................................ 51
      2.7.3 Speed ....................................... 51
   2.8 Color ........................................... 51
   2.9 Pixel sharing .................................... 53
2.10 Comparison between pixel architecture ........................... 55
2.11 Comparison with CCDs .............................................. 55

3 Smart functions and materials ........................................ 59
  3.1 Introduction ......................................................... 59
  3.2 Pixel structure ..................................................... 60
    3.2.1 Current mode .................................................. 60
    3.2.2 Log sensor ..................................................... 62
  3.3 Analog operation .................................................. 64
    3.3.1 Winner-take-all .............................................. 64
    3.3.2 Projection ..................................................... 65
    3.3.3 Resistive network ............................................ 65
  3.4 Pulse modulation .................................................. 66
    3.4.1 Pulse width modulation .................................... 68
    3.4.2 Pulse frequency modulation ................................ 70
  3.5 Digital processing ................................................ 78
  3.6 Materials other than silicon .................................... 79
    3.6.1 Silicon-on-insulator ....................................... 79
    3.6.2 Extending the detection wavelength ........................ 83
  3.7 Structures other than standard CMOS technologies .............. 85
    3.7.1 3D integration .............................................. 85
    3.7.2 Integration with light emitters ............................ 86
    3.7.3 Color realization using nonstandard structures .......... 88

4 Smart imaging .......................................................... 93
  4.1 Introduction ......................................................... 93
  4.2 Low light imaging ................................................ 94
    4.2.1 Active reset for low light imaging ......................... 96
    4.2.2 PFM for low light imaging ................................. 96
    4.2.3 Differential APS ........................................... 97
    4.2.4 Geiger mode APD for a smart CMOS image sensor .......... 97
  4.3 High speed .......................................................... 99
    4.3.1 Global shutter ............................................... 99
  4.4 Wide dynamic range ............................................... 100
    4.4.1 Principle of wide dynamic range ............................ 100
    4.4.2 Dual sensitivity ............................................ 101
    4.4.3 Nonlinear response ......................................... 102
    4.4.4 Multiple sampling ......................................... 105
    4.4.5 Saturation detection ....................................... 107
    4.4.6 Diffusive brightness ..................................... 108
  4.5 Demodulation ....................................................... 108
    4.5.1 Principles of demodulation ................................ 108
    4.5.2 Correlation .................................................. 109
    4.5.3 Method of two accumulation regions ....................... 111
  4.6 Three-dimensional range finder .................................. 116

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1

Introduction

1.1 A general overview

Complementary metal-oxide-semiconductor (CMOS) image sensors have been the subject of extensive development and now share the market with charge coupled device (CCD) image sensors, which have dominated the field of imaging sensors for a long time. CMOS image sensors are now widely used not only for consumer electronics, such as compact digital still cameras (DSC), mobile phone cameras, handycamcorders, and digital single lens reflex (DSLR) cameras, but also for cameras used for automobiles, surveillance, security, robot vision, etc. Recently, further applications of CMOS image sensors in biotechnology and medicine have emerged. Many of these applications require advanced performance such as wide dynamic range, high speed, and high sensitivity, while others need dedicated functions, such as real time target tracking and three-dimensional range finding. It is difficult to perform such tasks with conventional image sensors. Furthermore, some signal processing devices are insufficient for these purposes. Smart CMOS image sensors, CMOS image sensors with integrated smart functions on the chip, may meet the requirements of these applications.

CMOS image sensors are fabricated based on standard CMOS large scale integration (LSI) fabrication processes, while CCD image sensors are based on a specially developed fabrication process. This feature of CMOS image sensors makes it possible to integrate functional circuits to develop smart CMOS image sensors and to realize both a higher performance than that of CCDs and conventional CMOS image sensors and versatile functions that cannot be achieved with conventional image sensors.

Smart CMOS image sensors are mainly aimed at two different fields. One is the enhancement or improvement of the fundamental characteristics of CMOS image sensors, such as dynamic range, speed, and sensitivity. Another is the implementation of new functions, such as three-dimensional range finding, target tracing, and modulated light detection. For both fields, many architectures and/or structures, as well as materials, have been proposed and demonstrated.

The following terms are also associated with smart CMOS image sensors: computational CMOS image sensors, integrated functional CMOS image sensors, vision chips, focal plane image processing, as well as many others. Besides vision chips, these terms suggest that an image sensor has other functions in addition to imaging.
The name vision chip originates from a device proposed and developed by C. Mead and coworkers, which mimics the human visual system. It will be described later in this chapter. In the following section, we survey the history of CMOS image sensors and then review the brief history of smart CMOS image sensors.

1.2 Brief history of CMOS image sensors

The birth of MOS imagers

The history of MOS image sensors, shown in Fig. 1.1, starts with solid-state imagers used as a replacement for image tubes. For solid-state image sensors, four important functions had to be realized: light-detection, accumulation of photo-generated signals, switching from accumulation to readout, and scanning. These functions are discussed in Chapter 2. The scanning function in X–Y addressed silicon-junction photosensing devices was proposed in the early 1960s by S.R. Morrison at Honeywell as the “photoscanner” [9] and by J.W. Horton et al. at IBM as the “scansion” [10]. P.K. Weimer et al. proposed solid-state image sensors with scanning circuits using thin-film transistors (TFTs) [11]. In these devices, photoconductive film, discussed in Sec. 2.3.5, is used for the photodetector. M.A. Schuster and G. Strull at NASA used phototransistors (PTrs), which are discussed in Section 2.3.3, as photodetectors, as well as switching devices to realize X–Y addressing [12]. They successfully obtained images with a fabricated 50 × 50-pixel array sensor.

The accumulation mode in a photodiode is an important function for MOS image sensors and is described in Section 2.4. It was first proposed by G.P. Weckler at Fairchild Semiconductor [13]. In the proposal, the floating source of a MOSFET is used as a photodiode. This structure is used in some present CMOS image sensors. Weckler later fabricated and demonstrated a 100 × 100-pixel image sensor using this structure [14]. Since then, several types of solid-state image sensors have been proposed and developed [14–17], as summarized in Ref. [18].

The solid-state image sensor developed by P.J. Noble at Plessey was almost the same as a MOS image sensor or passive pixel sensor (PPS), discussed in Section 2.5.1, consisting of a photodiode and a switching MOS transistor in a pixel with X- and Y-scanners and a charge amplifier. Noble briefly discussed the possibility of integrating logic circuitry for pattern recognition on a chip, which may be the first prediction of a smart CMOS image sensor.

Competition with CCDs

Shortly after the publication of details of solid-state sensors in IEEE Transaction on Electron Devices in 1968, CCD image sensors appeared [19]. The CCD itself was invented in 1969 by W. Boyle and G.E. Smith at AT&T Bell Laboratories [19] and was experimentally verified at almost the same time [20]. Initially, the CDD was
developed as semiconductor bubble memory, as a replacement for magnetic bubble memory, but was soon developed for use in image sensors. The early stages of the invention of the CCD is described in Ref. [21].

Considerable research effort resulted in the production of the first commercial MOS imagers, appearing in the 1980s [22–27]. While Hitachi and Matsushita have developed MOS imagers [28], until recently CCDs have been widely manufactured and used due to the fact that they have offered superior image quality than MOS imagers.

Solid-state imagers with in-pixel amplification

Subsequently, effort has been made to improve the signal-to-noise ratio (SNR) of MOS imagers by incorporating an amplification mechanism in a pixel. In the 1960s, a phototransistor (PTr) type imager was developed [12]. In the late 1980s, several amplified type imagers were developed, including the charge modulated device (CMD) [29], floating gate array (FGA) [30], base-stored image sensor (BASIS) [31], static induction transistor (SIT) type [32], amplified MOS imager (AMI) [33–37], and others [6, 7]. Apart from AMI, these required some modification of standard
MOS fabrication technology in the pixel structure, and ultimately they were not commercialized and their development was terminated. AMI can be fabricated in standard CMOS technology without any modification, however, and its pixel structure is the same as that of the active pixel sensor (APS); although AMI uses an I–V converter as a readout circuit while APS uses a source follower, though this difference is not critical. APS is also classified as an image sensor with in-pixel amplification.

Present CMOS image sensors

APS was first realized by using a photogate (PG) as a photodetector by E. Fossum et al. at JPL* and then by using a photodiode (PD) [38, 39]. A PG was used mainly due to ease of signal charge handling. The sensitivity of a PG is not as good since polysilicon as a gate material is opaque at the visible wavelength region. APSs using a PD are called 3T-APSs (three transistor APSs) and are now widely used in CMOS image sensors. In the first stage of 3T-APS development, the image quality could not compete with that of CCDs, both with respect to fixed pattern noise (FPN) and random noise. Introducing noise canceling circuits reduces FPN but not random noise.

By incorporating a pinned PD structure used in CCDs, which has a low dark current and complete depletion structure, the 4T-APS (four transistor APS) has been successfully developed [40]. A 4T-APS can be used with correlated double sampling (CDS), which can eliminate $k_b T C$ noise, the main factor in random noise. The image quality of 4T-APSs can compete with that of CCDs. The final issue for 4T-APSs is the large pixel size compared with that in CCDs. A 4T-APS has four transistors plus a PD and floating diffusion (FD) in a pixel, while a CCD has one transfer gate plus a PD. Although CMOS fabrication technology advances have benefited the development of CMOS image sensors [41], namely in shrinking the pixel size, it is essentially difficult to realize a smaller pixel size than that of CCDs. Recently, a pixel sharing technique has been widely used in 4T-APSs and has been effective in reducing the pixel size to be comparable with that of CCDs. Figure 1.2 shows the trend of pixel pitch in 4T-APSs. The figure illustrates that the pixel pitch of CMOS image sensors is comparable with that of CCDs, shown as open squares in the figure.

*Jet Propulsion Laboratory.
1.3 Brief history of smart CMOS image sensors

Vision chips

There are three main categories for smart CMOS image sensors, as shown in Fig. 1.3: pixel-level processing, chip-level processing or camera-on-a-chip, and column-level processing. The first category is vision chips or pixel-parallel processing. In the 1980s, C. Mead and coworkers at Caltech * proposed and demonstrated vision chips or silicon retina [42]. A silicon retina mimics the human visual processing system with massively parallel-processing capability using Si LSI technology. The circuits work in the subthreshold region, as discussed in Appendix E, in order to achieve low power consumption. In addition, the circuits automatically execute to solve a given problem by using convergence in two-dimensional resistive networks, as described in Section 3.3.3. They frequently use phototransistors (PTrs) as photodetectors due to the gain of PTrs. Since the 1980s, considerable work has been done on developing visions chips and similar devices, as reviewed by Koch and Liu [43], and A. Moini [1]. Massively parallel processing in the focal plane is very attractive and has been the subject of much research into fields such as programmable artificial retinas [44]. Some applications have been commercialized, such as two-layered resistive networks using 3T-APS by T. Yagi, S. Kameda, and co-workers at Osaka Univ. [45, 46].

*California Institute of Technology.
FIGURE 1.3
Three types of smart sensors.

FIGURE 1.4
ITRS roadmap; the trend of DRAM half pitch [47].

Figure 1.4 shows the LSI roadmap of ITRS* [47]. This figure shows the trend

*International Technology Roadmap for Semiconductors.
of dynamic random access memory (DRAM) half pitch; other technologies such as logic processes exhibit almost the same trend, namely the integration density of LSI increases according to Moore’s law such that the integration density doubles every 18—24 months [48].

This advancement of CMOS technology means that massively parallel processing or pixel-parallel processing is becoming more feasible. Considerable research has been published, such as vision chips based on cellular neural networks (CNN) [49–52], programmable multiple instruction and multiple data (MIMD) vision chips [53], biomorphic digital vision chips [54], and analog vision chips [55, 56]. Other pioneering work include digital vision chips using pixel-level processing based on a single instruction and multiple data (SIMD) processor by M. Ishikawa et al. at Univ. Tokyo and Hamamatsu Photonics [57–63].

It is noted that some vision chips are not based on the human visual processing system, and thus they belong in the category of pixel-level processing.

**Advancement of CMOS technology and smart CMOS image sensors**

The second category, pixel-level programming, is more tightly related with the advancement of CMOS technology and has little relation with pixel-parallel processing. This category includes system-on-chip and system-on-a-camera. In the early 1990s, advancement of CMOS technology made it possible to realize highly integrated CMOS image sensors or smart CMOS image sensors for machine vision. Pioneering work include ASIC vision (originally developed in Univ. Edinburgh [64,65] and later by VLSI Vision Ltd. (VVL), near-sensor image processing (NSIP) (later known as PASIC [66]) originally developed in Linköping University [67] and MAPP by Integrated Vision Products (IVP) [68].

PASIC may be the first CMOS image sensor that uses a column level analog-to-digital converter (ADC) [66]. ASIC vision has a PPS structure [67], while NSIP uses a pulse width modulation (PWM) based sensor [67], discussed in Section 3.4.1. MAPP uses an APS [68].

**Smart CMOS image sensors based on high performance CMOS image sensor technologies**

Some of the above mentioned sensors have column-parallel processing structure, the third of the categories. Column-parallel processing is suitable for CMOS image sensors, because the column lines are electrically independent of each other. Column-parallel processing can enhance the performance of CMOS image sensors, such as widening the dynamic range and increasing the speed. Combining with 4T-APSs, column-parallel processing exhibit a high image quality and versatile functions. Therefore, recently column-level processing architecture has been widely used for higher performance CMOS image sensors. The advancement of LSI technologies also broadens the range of applications of this architecture.
1.4 Organization of the book

This book is organized as follows. First, in this introduction, a general overview of solid-state image sensors is presented. Then, smart CMOS image sensors are described including a brief history and a discussion of their features. Next, in Chapter 2, fundamental information on CMOS image sensors is presented in detail. First, optoelectronic properties of silicon semiconductors, based on CMOS technology, are described in Section 2.2. Then, in Section 2.3, several types of photodetectors are introduced, including the photodiode, which is commonly used in CMOS image sensors. The operation principle and fundamental characteristics of photodiodes are described. In a CMOS image sensor, a photodiode is used in the accumulation mode, which is very different from the mode of operation for other applications such as optical communication. The accumulation mode is discussed in Section 2.4. Pixel structure is the heart of this chapter and is explained in Section 2.5 for active pixel sensors (APS) and passive pixel sensors (PPS). Peripheral blocks other than pixels are described in Section 2.6. Addressing and readout circuits are also mentioned in that section. The fundamental characteristics of CMOS image sensors are discussed in Section 2.7. The topics of color (Section 5.4.1) and pixel sharing (Section 2.9) are also described in this chapter. Finally, several comparisons are discussed in Sections 2.10 and 2.11.

In Chapter 3, several smart functions and materials are introduced. Certain smart CMOS image sensors have been developed by introducing new functions into conventional CMOS image sensor architecture. Firstly, pixel structures different from that of conventional APS are introduced in Section 3.2, such as the log sensor. Smart CMOS image sensors can be classified into three categories, analog, digital, and pulse, described in Sections 3.3, 3.4, and 3.5. CMOS image sensors are typically based on silicon CMOS technologies, but other technologies and materials can be used to achieve smart functions. For example, silicon on sapphire (SOS) technology is a candidate for smart CMOS image sensors. Section 3.6 discussed materials other than silicon in smart CMOS image sensors. Structures other than standard CMOS technologies are described in Section 3.7.

By combining the smart functions introduced in Chapter 3, Chapter 4 describes several examples of smart imaging. Low-light imaging (Section 4.2), high speed (Section 4.3), and wide dynamic range (Section 4.4) are presented with examples. These features of smart CMOS image sensors give a higher performance compared with conventional CMOS image sensors. Another feature of smart CMOS image sensors is to achieve versatile functions that cannot be realized by conventional image sensors. For this, sections on demodulation (Section 4.5), three-dimensional range finders (Section 4.6), and target tracking (Section 4.7) are presented. Finally in this chapter, dedicated arrangements of pixels and optics are described. Section 4.8 considers two types of smart CMOS image sensors with nonorthogonal pixel arrangements and dedicated optics.

The final chapter, Chapter 5, considers applications using smart CMOS image
Introduction

sensors in the field of information and communication technologies, biotechnologies, and medicine. These applications have recently emerged and will be important for the next generation of smart CMOS image sensors.

Several appendices are attached to present additional information for the main body of the book.
2

Fundamentals of CMOS image sensors

2.1 Introduction

This chapter provides the fundamental knowledge for understanding CMOS image sensors.

A CMOS image sensor generally consists of an imaging area, which consists of an array of pixels, vertical and horizontal access circuitry, and readout circuitry, as shown in Fig. 2.1.

![Architecture of a CMOS image sensor](image.png)

**FIGURE 2.1**
Architecture of a CMOS image sensor. A two-dimensional array of pixels, vertical and horizontal access circuitry, and readout circuitry are generally implemented. A pixel consists of a photodetector and transistors.

The imaging area is a two-dimensional array of pixels; each pixel contains a photodetector and some transistors. This area is the heart of an image sensor and the imaging quality is largely determined by the performance of this area. Access circuitry is used to access a pixel and read the signal value in the pixel. Usually a
scanner or shift register is used for the purpose, and a decoder is used to access pixels randomly, which is sometimes important for smart sensors. A readout circuit is a one-dimensional array of switches and a sample and hold (S/H) circuit. Noise cancel circuits, such as correlated double sampling (CDS), are employed in this area.

In this chapter, these fundamental elements of CMOS image sensors are described. First, photodetection is explained. The behavior of minority carriers plays an important role in photodetection. Several kinds of photodetectors for CMOS image sensors have been introduced. Among them, pn-junction photodiodes are most often used, and the operation principle and hence the basic characteristics of pn-junction photodiodes are explained here in detail. In addition, the accumulation mode, which is an important operation for CMOS image sensors, is described. Then, basic pixel structures are introduced, namely passive pixel sensors and active pixel sensors. Finally, further elements for CMOS image sensors are described, such as scanners and decoders, read-out circuits, and noise cancellers.

### 2.2 Fundamentals of photodetection

#### 2.2.1 Absorption coefficient

When light is incident on a semiconductor, a part of the incident light is reflected while the rest is absorbed in the semiconductor and produces electron–hole pairs inside the semiconductor, as shown in Fig. 2.2. Such electron–hole pairs are called photo-generated carriers. The amount of photo-generated carriers depends on the semiconductor material and is described by the absorption coefficient $\alpha$.

It should be noted that $\alpha$ is defined as the ratio of decrease of light power $\Delta P / P$ when the light travels a distance $\Delta z$, that is,

$$\alpha(\lambda) = \frac{1}{\Delta z} \frac{\Delta P}{P}. \quad (2.1)$$

From Eq. 2.1, the following relation is derived:

$$P(z) = P_0 \exp(-\alpha z). \quad (2.2)$$

The absorption length $L_{abs}$ is defined as

$$L_{abs} = \alpha^{-1}. \quad (2.3)$$

It is noted that the absorption coefficient is a function of photon energy $h \nu$ or wavelength $\lambda$, where $h$ and $\nu$ are Planck’s constant and the frequency of the light. The value of the absorption length $L_{abs}$ thus depends on wavelength. Figure 2.3 shows the dependence of the absorption coefficient and the absorption length of silicon on the input light wavelength. In the visible region, 0.4–0.6 $\mu$m, the absorption length lies within 0.1–10 $\mu$m [69]. The absorption length is an important figure for a rough estimation of a photodiode structure.
2.2.2 Behavior of minority carriers

Incident light on a semiconductor generates electron–hole pairs or photo-generated carriers. When electrons are generated in a p-type region, the electrons are minority carriers. The behavior of minority carriers is important for image sensors. For example, in a CMOS image sensor with a p-type substrate, photo-generated minority carriers in the substrate are electrons. This situation occurs when infrared (IR) light is incident in the sensor, because the absorption length in the IR region is over 10 μm, as shown in Fig. 2.3, and thus the light reaches the substrate. In that case, the diffusion behavior of the carriers greatly affects the image sensor characteristics; they can diffuse to adjacent photodiodes through the substrate and cause image blurring. To suppress this, an IR cut filter is usually used, because IR light reaches deeper regions of the photodiode, namely the substrate, and produces more carriers than visible light in the deeper regions.

The mobility and lifetime of minority carriers are empirically given by the following relations [70–72] with parameters of acceptor concentration $N_a$ and donor concentration $N_d$:

$$\mu_n = 233 + \frac{1180}{1 + [N_a/(8 \times 10^{16})]^{0.9}} \text{ [cm}^2/\text{V} \cdot \text{s]}, \quad (2.4)$$

$$\mu_p = 130 + \frac{370}{1 + [N_d/(8 \times 10^{17})]^{1.25}} \text{ [cm}^2/\text{V} \cdot \text{s]}, \quad (2.5)$$

$$\tau_n^{-1} = 3.45 \times 10^{-12} N_a + 0.95 \times 10^{-31} N_a^2 \text{ [s}^{-1}], \quad (2.6)$$
FIGURE 2.3
Absorption coefficient (solid line) and absorption length (broken line) of silicon as a function of wavelength. From the data in [69].

\[ \tau_p^{-1} = 7.8 \times 10^{-13} N_a + 1.8 \times 10^{-31} N_d^2 \text{ [s}^{-1}] \]  

(2.7)

From the above equations, we can estimate the diffusion lengths \( L_{n,p} \) for electrons and holes by using the relation

\[ L_{e,p} = \sqrt{\frac{k_B T \mu_{n,p} \tau_{n,p}}{e}}. \]  

(2.8)

Figure 2.4 shows the diffusion lengths of electrons and holes as a function of impurity concentration. Note that both electrons and holes can travel over 100 \( \mu \text{m} \) for impurity concentrations below \( 10^{17} \text{ cm}^{-3} \).
2.2.3 Sensitivity and quantum efficiency

The sensitivity is defined as the amount of photocurrent $I_L$ produced when a unit of light power $P_o$ is incident on a material. It is given by

$$R_{ph} = \frac{I_L}{P_o}$$

(2.9)
The quantum efficiency is defined as the ratio of the number of generated photocarriers to the number of the input photons. The input photon number per unit time and the generated carrier number per unit time are $I_L/e$ and $P_e/(h\nu)$, and thus the quantum efficiency is expressed as

$$\eta_Q \equiv \frac{I_L/e}{P_e/(h\nu)} = \frac{R_{ph}}{e}.$$  \hspace{1cm} (2.10)

From Eq. 2.10, the maximum sensitivity, that is the sensitivity at $\eta_Q = 1$, is found to be

$$R_{ph,max} = \frac{e}{h\nu} = \frac{e}{hc} \lambda = \frac{\lambda [\mu m]}{1.23}.$$ \hspace{1cm} (2.11)

$R_{ph,max}$ is illustrated in Fig. 2.6. It monotonically increases in proportion to the wavelength of the input light and eventually reaches zero at the wavelength $\lambda_g$ corresponding to the bandgap of the material $E_g$. For silicon, the wavelength is about 1.12 $\mu$m since the bandgap of silicon is 1.107 eV.

![Figure 2.6](image-url)
2.3 Photodetectors for smart CMOS image sensors

Most photodetectors used in CMOS image sensors are pn-junction photodiodes (PDs). In the next sections, PDs are described in detail. Other photodetectors used in CMOS image sensors are photogates (PGs), phototransistors (PTrs), and avalanche photodiodes (APDs). PTrs and APDs both make use of gain; another detector with gain is the photoconductive detector (PCD). Figure 2.7 illustrates the structures of PDs, PGs, and PTrs.

FIGURE 2.7
Symbols and structures of (a) photodiode, (b) photogate, (c) vertical type phototransistor, and (d) lateral type phototransistor.
2.3.1 pn-junction photodiode

In this section, a conventional photodetector, a pn-junction PD, is described [73, 74]. First, the operation principle of a PD is described and then several fundamental characteristics, such as quantum efficiency, sensitivity, dark current, noise, surface recombination, and speed, are discussed. These characteristics are important for smart CMOS image sensors.

2.3.1.1 Operation principle

The operation principle of the pn-junction PD is quite simple. In a pn-junction diode, the forward current $I_F$ is expressed as

$$I_F = I_{diff} \left[ \exp \left( \frac{eV}{nk_BT} \right) - 1 \right],$$

(2.12)

where $n$ is an ideal factor and $I_{diff}$ is the saturation current or diffusion current, which is given by

$$I_{diff} = eA \left( \frac{D_n}{L_n} n_{po} + \frac{D_p}{L_p} p_{no} \right),$$

(2.13)

where $D_n, D_p, L_n, L_p, n_{po}$, and $p_{no}$ are the diffusion coefficient, diffusion length, minority carrier concentration in the p-type region, and the minority carrier concentration in n-type region, respectively. $A$ is the cross-section area of the pn-diode. The photocurrent of the pn-junction photodiode is expressed as follows:

$$I_L = I_{ph} - I_F$$

$$= I_{ph} - I_{diff} \left[ \exp \left( \frac{eV}{nk_BT} \right) - 1 \right],$$

(2.14)

where $n$ is an ideal factor. Figure 2.8 illustrates the I–V curves of a pn-PD under dark and illuminated conditions. There are three modes for bias conditions: solar cell mode, PD mode, and avalanche mode, as shown in Fig. 2.8.

**Solar cell mode** In the solar cell mode, no bias is applied to the PD. Under light illumination, the PD acts as a battery, that is it produces a voltage across the pn-junction. Figure 2.8 shows the open circuit voltage $V_{oc}$. In the open circuit condition, the voltage $V_{oc}$ can be obtained from $I_L = 0$ in Eq. 2.14, and thus

$$V_{oc} = \frac{k_BT}{e} \ln \left( \frac{I_{ph}}{I_{diff}} + 1 \right).$$

(2.15)

This shows that the open circuit voltage does not linearly increase according to the input light intensity.
PD mode  The second mode is the PD mode. When a PD is reverse biased, that is $V < 0$, the exponential term in Eq. 2.14 can be neglected, and thus $I_L$ becomes

$$I_L \approx I_{ph} + I_{diff}.$$  \hspace{1cm} (2.16)

This shows that the output current of the PD is equal to the sum of the photocurrent and diffusion current. Thus, the photocurrent lineally increases according to the input light intensity.

Avalanche mode  The third mode is the avalanche mode. When a PD is strongly biased, the photocurrent suddenly increases, as shown in Fig. 2.8. This phenomena is called an avalanche, where impact ionization of electrons and holes occurs and the carriers are multiplied. The voltage where an avalanche occurs is called the avalanche breakdown voltage $V_{bd}$, shown in Fig. 2.8. Avalanche breakdown is explained in Sec. 2.3.1.3. The avalanche mode is used in an avalanche photodiode (APD) and is described in Sec. 2.3.4.
2.3.1.2 Quantum efficiency and sensitivity

By using the definition of the absorption coefficient in Eq. 2.2 $\alpha(\lambda)$, the light intensity is expressed as

$$dP(z) = -\alpha(\lambda) P_0 \exp[-\alpha(\lambda) z] dz.$$  \hspace{1cm} (2.17)

To make it clear that the absorption coefficient is dependent on the wavelength, $\alpha$ is written as $\alpha(\lambda)$. The quantum efficiency is defined as the ratio of absorbed light intensity to the total input light intensity, and thus

$$\eta_Q = \frac{\int_{x_p}^{x_n} \alpha(\lambda) P_0 \exp[-\alpha(\lambda) x] \, dx}{\int_{0}^{\infty} \alpha(\lambda) P_0 \exp[-\alpha(\lambda) x] \, dx} = \left(1 - \exp[-\alpha(\lambda) W]\right) \exp[-\alpha(\lambda) x_n],$$  \hspace{1cm} (2.18)

where $W$ is the depletion width and $x_n$ is the distance from the surface to the edge of the depletion region as shown in Fig. 2.9.

**FIGURE 2.9**

pn-junction structure. The junction is formed at a position $x_j$ from the surface. The depletion region widens at the sides of the n-type region $x_n$ and p-type region $x_p$. The width of the depletion region $W$ is thus equal to $x_n - x_p$.

Using Eq. 2.18, the sensitivity is expressed as follows:

$$R_{ph} = \eta_Q \frac{e\lambda}{hc} = \frac{e\lambda}{hc} \left(1 - \exp[-\alpha(\lambda) W]\right) \exp[-\alpha(\lambda) x_n].$$  \hspace{1cm} (2.19)

In this equation, the depletion width $W$ and the part of the depletion width at the N region $x_n$ are expressed as follows. Using the built-in potential $V_{bi}$, $W$ under an applied voltage $V_{appl}$ is expressed as

$$W = \sqrt{\frac{2eSi(N_d + N_a)(V_{bi} + V_{appl})}{eN_aN_d}},$$  \hspace{1cm} (2.20)
where $\varepsilon_{Si}$ is the dielectric constant of silicon. The built-in potential $V_{bi}$ is given by

$$V_{bi} = k_B T \ln \left( \frac{N_d N_a}{n_i^2} \right),$$

(2.21)

where $n_i$ is the intrinsic carrier concentration for silicon and $n_i = 1.4 \times 10^{10}$ cm$^{-3}$.

The parts of the depletion width at the n-region and p-region are

$$x_n = \frac{N_a}{N_a + N_d} W,$$

(2.22)

$$x_p = \frac{N_d}{N_a + N_d} W.$$  

(2.23)

Figure 2.6 shows the sensitivity spectrum curve of silicon, that is, the dependence of the sensitivity on the input light wavelength. The sensitivity spectrum curve is dependent on the impurity profile of the n-type and p-type regions as well as the position of the pn-junction $x_j$. In the calculation of the curve in Fig. 2.6, the impurity profile in both the n-type and p-type regions is flat and the junction is abrupt. In addition, only photo-generated carriers in the depletion region are accounted for; some portion of the photo-generated carriers outside the depletion region diffuse and reach the depletion region, but in the calculation these diffusion carriers are not accounted for. Such diffusion carriers can affect the sensitivity at long wavelengths because of the low value of the absorption coefficient in the long wavelength region [75]. Another assumption is to neglect the surface recombination effect, which will be considered in the section on noise, Sec. 2.3.1.4. These assumptions will be discussed in Sec. 2.4. An actual PD in an image sensor is coated with SiO$_2$ and Si$_3$N$_4$, and thus the quantum efficiency is changed [76].

2.3.1.3 Dark current

Dark current in PDs has several sources.

**Diffusion current** The diffusion current inherently flows and is expressed as

$$I_{diff} = A e \left( \frac{D_n p_w}{L_n} + \frac{D_p n_w}{L_p} \right)$$

$$= A e \left( \frac{D_n}{L_n N_a} + \frac{D_p}{L_p N_d} \right) N_c N_v \exp \left( -\frac{E_g}{k_B T} \right),$$

(2.24)

where $A$ is the diode area, $N_c$ and $N_v$ are the effective density of states in the conduction band and valence band, respectively, and $E_g$ is the bandgap. Thus, the diffusion current exponentially increases as the temperature increases. It is noted that the diffusion current weakly depends on the bias voltage; more precisely, it depends on the square root of the bias voltage.
Dependence of the sensitivity (solid line) and quantum efficiency (broken line) of a pn-junction PD on wavelength. The PD parameters are summarized in the inset.

**Tunnel current** Other dark currents include tunnel current, generation–recombination (g–r current), Frakel–Poole current, and surface leak current [77,78]. The tunnel current consists of band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT), which has an exponential dependence on the bias voltage [77–79] but has little dependence on the temperature. Although both BTBT and TAT cause dark current exponentially dependent on bias voltage, the dependence is different, as shown in Table 2.1. The tunnel current is important when doping is large and thus the depletion width becomes thin so as to lead to tunneling.

**G–R current** In the depletion region, the carrier concentration is reduced and carrier generation occurs rather than recombination of carriers [77,80] by thermal generation. This causes dark current. The g–r current is given by [77]

\[
I_{gr} = AW \frac{e n_i}{\tau_g} = AW e \frac{\sqrt{N_c N_v}}{\tau_g} \exp \left( - \frac{E_g}{2k_B T} \right),
\]

where \( W \) is the depletion width, \( \tau_g \) is the lifetime of the deep level, and \( n_i \) is the intrinsic carrier concentration. This process is called Shockley–Read–Hall recombi-
Impact ionization current  Impact ionization or avalanche breakdown increases dark current when the bias voltage increases [81, 82]. The bias dependence of dark current by impact ionization arises from the voltage dependence of the ionization coefficients of electrons and holes, \( \alpha_n \) and \( \alpha_p \). These coefficients exponentially increase by as the bias voltage increases.

Frankel–Poole current  The Frankel–Poole current originates from the emission of trapped electrons into the conduction band [77]. This current strongly depends on the bias voltage, which is the same as the tunneling current.

Surface leak current  The surface leak current is given by

\[
I_{\text{surf}} = \frac{1}{2} e n_i s_0 A_s,
\]  

\[ (2.26) \]

where \( n_i \), \( s_0 \), and \( A_s \) are the intrinsic carrier concentration, surface recombination rate, and surface area, respectively.

---

TABLE 2.1

<table>
<thead>
<tr>
<th>Process</th>
<th>Dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion</td>
<td>( \propto \exp \left( \frac{-E_d}{kT} \right) )</td>
</tr>
<tr>
<td>G–R</td>
<td>( \propto \sqrt{V}\exp \left( \frac{-E_d}{2kT} \right) )</td>
</tr>
<tr>
<td>Band-to-band tunneling</td>
<td>( \propto V^2 \exp \left( \frac{-a V}{kT} \right) )</td>
</tr>
<tr>
<td>Trap-assisted tunneling</td>
<td>( \propto \exp \left( \frac{-a' V}{kT} \right)^2 )</td>
</tr>
<tr>
<td>Impact ionization</td>
<td>( \propto \exp \left( \frac{-b V}{kT} \right) )</td>
</tr>
<tr>
<td>Frankel–Poole</td>
<td>( \propto V \exp \left( \frac{-c T}{k} \right) )</td>
</tr>
<tr>
<td>Surface leak</td>
<td>( \propto \exp \left( \frac{-E_a}{2kT} \right) )</td>
</tr>
</tbody>
</table>
Dependence of dark current on temperature and bias voltage

Comparing Eqs. 2.24, 2.25, and 2.26 shows that the temperature dependences of the various dark currents are different; only \( I_{\text{surf}} \) is independent of temperature, while \( \log I_{\text{diff}} \) and \( \log I_{\text{gr}} \) vary as \(-\frac{1}{T}\) and \(-\frac{1}{2T}\), respectively. Thus, the temperature dependence can reveal the origin of the dark current. Also, the dependence on the bias voltage is different. The dependence on temperature and bias voltage is summarized in Table 2.1.

2.3.1.4 Noise

Shot noise

A PD suffers from shot noise and thermal noise. Shot noise originates from fluctuations in the number of the particles \( N \) such as electrons and photons. Thus shot noise and electron (or hole) shot noise inherently exist in a PD. The root mean square of the shot noise current \( i_{\text{sh}} \) is expressed as

\[
    i_{\text{sh, rms}} = \sqrt{2eI\Delta f},
\]

where \( T \) and \( \Delta f \) indicate average signal current and bandwidth, respectively. The signal-to-noise ratio (SNR) for shot noise is expressed as

\[
    \text{SNR} = \frac{T}{\sqrt{2eI\Delta f}} = \frac{\sqrt{T}}{2e\Delta f}.
\]

Thus, as the amount of current or the number of electrons decreases, the SNR associated with shot noise decreases. Dark current also produces shot noise.

Thermal noise

In a load resistance \( R \), free electrons exist and randomly move according to the temperature of the load resistance. This effect generates thermal noise, also known as Johnson noise or Nyquist noise. The thermal noise is expressed as

\[
    i_{\text{sh, rms}} = \sqrt{\frac{4k_BT\Delta f}{R}}.
\]

In CMOS image sensors, the thermal noise appears as \( k_BT/C \) noise, which is discussed in Sec. 2.7.1.2.

2.3.1.5 Surface recombination

In a conventional CMOS image sensor, the surface of the silicon is interfaced with \( \text{SiO}_2 \) and has some dangling bonds, which produce surface states or interface states acting as non-recombination centers. Some photo-generated carriers near the surface are trapped at the centers and do not contribute to the photocurrent. Thus these surface states degrade the quantum efficiency or sensitivity. This effect is called surface recombination. The feature parameter for surface recombination is the surface recombination velocity \( S_{\text{surf}} \). The surface recombination rate is proportional to the excess carrier density at the surface:

\[
    D_n \frac{\partial n_p}{\partial x} = S_{\text{surf}} [n_p(0) - n_{po}].
\]
The recombination velocity is strongly dependent on the interface state, band bending, defects, and other effects, and is approximately 10 cm$^3$/sec for both electrons and holes. For short wavelengths, such as blue light, the absorption coefficient is large and absorption mostly occurs at the surface. Thus it is important to reduce the surface recombination velocity to achieve high quantum efficiency in the short wavelength region.

### 2.3.1.6 Speed

In the recent growth of optical fiber communications and fiber-to-the-home (FTTH) technology, silicon CMOS photoreceivers have been extensively studied and developed. High-speed photodetectors using CMOS technologies, including BiCMOS technology, are described in detail in Ref. [83, 84], and high-speed circuits for CMOS optical fiber communication are also detailed in Ref. [85].

In conventional image sensors, the speed of the PD is not a concern. However, some kinds of smart image sensors need a PD with a fast response. Smart CMOS sensors for optical wireless LANs is an example and is considered in Chapter 5; they are based on technologies for CMOS-based photoreceivers for optical fiber communications, mentioned above. Another example is a smart CMOS sensor that can measure time-of-flight (TOF), also described in Chapter 5. In this case, an APD is used for its high-speed response.

Here we consider the response of a PD. Generally, the response of a PD is limited by the CR time constant $\tau_{CR}$, transit time $\tau_{tr}$, and diffusion time of minority carriers $\tau_n$ for electrons:

- The CR time originates from the pn-junction capacitance $C_D$ and is expressed as
  $$\tau_{CR} = 2\pi C_D R_L,$$
  (2.31)
  where $R_L$ is the load resistance.

- The transit time is defined as the time for a carrier to drift across the depletion region. It is expressed as
  $$\tau_{tr} = W/v_s,$$
  (2.32)
  where $v_s$ is the saturation velocity.

- Minority carriers generated outside the depletion region can reach the depletion region after the diffusion time,
  $$\tau_{n,p} = \frac{L_n^2}{D_{n,p}},$$
  (2.33)
  for electrons with a diffusion coefficient of $D_n$.

It is noted there is a trade-off between depletion width $W$ and quantum efficiency $\eta_Q$ in the case of transit time limitation. In this case,

$$\eta_Q = [1 - \exp(-\alpha(\lambda)v_s\tau_{tr})] \exp(-\alpha(\lambda)x_n).$$
  (2.34)

Of these, the diffusion time has the greatest effect on the PD response in CMOS image sensors.
2.3.2 Photogate

The structure of a photogate (PG) is the same as a MOS capacitor; photo-generated carriers accumulate in the depletion region when the gate is biased. A PG has a suitable structure to accumulate and transfer carriers, and PGs have been used in some CMOS image sensors. The accumulation of photo-generated carriers in a PG is shown in Fig. 2.11. By applying a gate bias voltage, a depletion region is produced and acts as an accumulation region for photo-generated carriers, as shown in Fig. 2.11.

The fact that the photo-generated area is separated from the top surface in a PG is useful for some smart CMOS image sensors, as will be discussed in Chapter 5. It is noted that PGs have disadvantages with regard to sensitivity, because the gate, which is usually made of polysilicon, is partially transparent and has an especially low transmittance at shorter wavelength or in the blue light region.

![FIGURE 2.11](image)

Photogate structure with applied gate voltage, which produces a depletion region where photo-generated carriers accumulate.

2.3.3 Phototransistor

A phototransistor (PTr) can be made using standard CMOS technology for a parasitic transistor. A PTr amplifies a photocurrent by a factor of the base current gain $\beta$. Because the base width and carrier concentration are not optimized by standard
CMOS process technology, $\beta$ is not high, typically about 10–20. In particular, the base width is a trade-off factor for a phototransistor; when the base width increases, the quantum efficiency increases but the gain decreases [86]. Another disadvantage of a PTr is the large variation of $\beta$, which produces a fixed pattern noise (FPN), as detailed in Sec. 2.7.1.1. In spite of these disadvantages, PTrs are used in some CMOS image sensors due to their simple structure and their gain. When accompanied by current mirror circuits, PTrs can be used in current-mode signal processing, as discussed in Sec. 3.2.1. To address the low $\beta$ at low photocurrent, a vertical inversion-layer emitter pnp BJT structure has been developed [87].

2.3.4 Avalanche photodiode

An avalanche photodiode (APD) utilizes an avalanche effect in which photo-generated carriers are multiplied [86]. APDs have a gain as well as a high-speed response. APDs are thus used as detectors in optical fiber communication and ultra low light detection such as biotechnologies. However, they are hardly used in image sensors, because they require a high voltage over 100 V. Such a high voltage hinders the use of APDs in standard CMOS technologies besides hybrid image sensors with other APD materials with a CMOS readout circuit substrate, as reported in Ref. [88] for example. Gain variation causes the same problem as seen in PTrs.

Pioneering work by A. Biber et al. at Centre Suisse d’Electronique et de Microtechnique (CSEM) has produced a $12 \times 24$-pixel APD array fabricated in standard 1.2-$\mu$m BiCMOS technology [89]. Each pixel employs an APD control and readout circuits. An image is obtained with the fabricated sensor with an avalanche gain of about 7 under a bias voltage of 19.1 V.

Several reports have been published of APDs fabricated using standard CMOS technologies [90–100], as shown in Fig. 2.12. In these reports, the APD is biased over the avalanche breakdown voltage, and thus when photons are incident on the APD, it quickly turns on and produces a spike-like current pulse. This phenomenon resembles that of a Geiger counter and thus it is called the Geiger mode. The Geiger mode is difficult to use in imaging, though it can be used in another applications, as described in Chapter 5.

Recently, H. Finkelstein et al. at Univ. California, San Diego have reported a Geiger-mode APD fabricated in 0.18-$\mu$m CMOS technology [101]. They use shallow trench isolation (STI) as a guard ring for the APD. A bias voltage of 2.5 V is found to be sufficient to achieve avalanche breakdown. This result suggests that deep sub-micron technology can be used to fabricate a CMOS image sensor with a single photon avalanche diode (SPAD) pixel array.

2.3.5 Photoconductive detector

Another gain detector is the photoconductive detector (PCD), which uses the effect of photoconductivity [86]. A PCD typically has a structure of $n^+–n^-–n^+$. A DC bias is applied between the two $n^+$ sides, and thus the generated electric field is largely confined to the $n^-$ region, which is a photoconductive region where electron–hole
FIGURE 2.12
Avalanche photodiode structure using standard CMOS technology [98].

pairs are generated. The gain originates from a large ratio of the long lifetime of holes $\tau_p$ to the short transit time of electrons $t_{tr}$, that is $\tau_p \gg t_{tr}$. The gain $G_{pc}$ is expressed as

$$
G_{pc} = \frac{\tau_p}{t_{tr}} \left( 1 + \frac{\mu_p}{\mu_n} \right).
$$

(2.35)

When a photo-generated electron–hole pair is separated by an externally applied electric field, the electron crosses the detector several times before it recombines with the hole. It is noted that a larger gain results in a slower response speed, that is, the gain-bandwidth is constant in a PCD, because the gain $G_{pc}$ is proportional to the carrier lifetime $\tau_p$, which determines the response speed of the detector. Finally, a PCD has a relatively large dark current in general; as a PCD is essentially a conductive device, some dark current will flow. This may be disadvantage for an image sensor. Some PC materials are used as a detector overlaid on CMOS readout circuitry in a pixel due to the photoresponse with a variety of wavelengths such as X-ray, UV, and IR. Avalanche phenomena occur in some PC materials, realized in super HARP, an imaging tube with ultra high sensitivity developed in NHK [102].

Several types of CMOS readout circuitry (ROC) for this purpose have been reported, see Ref. [103] for example. Another application of PCD is as replacements for on-chip color filters, described in Sec. 3.7.3 [104–106]. Some PCDs are also used for fast photodetectors; metal–semiconductor–metal (MSM) photodetectors are used for this purpose.

Metal–semiconductor–metal photodetector The MSM photodetector is a kind of PCD, where a pair of metal fingers are placed on the surface of a semiconductor, as shown in Fig. 2.13 [86]. Because the MSM structure is easy to fabricate, MSM photodetectors are also applied to other materials such as GaAs and GaN. GaAs

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*Nippon Hoso Kyokai.*
MSM photodetectors are mainly used for ultra-fast photodetectors [107], although in Refs. [108, 109] GaAs MSM photodetector arrays are used for image sensors. GaN MSM photodetectors have been developed for image sensors with a sensitivity in the UV region [110].

![Structure of an MSM photodetector](image)

**FIGURE 2.13**
Structure of an MSM photodetector. The inset shows the symbols for the MSM photodetector.

### 2.4 Accumulation mode in PDs

A PD in a CMOS image sensor is usually operated in accumulation mode. In this mode, the PD is electrically floated and when light illuminates the PD, photocarriers are generated and swept to the surface due to the potential well in the depletion region. The PD accumulation mode was proposed and demonstrated by G.P. Weckler [13]. The potential voltage decreases when electrons accumulate. By measuring the voltage drop, the total amount of light power can be obtained. It should be noted that the accumulation of electrons is interpreted as the process of discharge in the charged capacitor by generated photocurrent.

Let us consider, using a simple but typical case, why the accumulation mode is required in a CMOS image sensor. We assume the following parameters: the sensitivity of the PD $R_{ph} = 0.3$ A/W, the area size of the PD $A = 1000$ lux, and the illumination at the PD surface $L_o = 100 \, \mu m^2$. Assuming that 1 lux roughly corresponds to $1.6 \times 10^{-7}$ W/cm$^2$, as described in the Appendix, the photocurrent $I_{ph}$ is...
evaluated as

\[ I_{ph} = R_{ph} \times L_0 \times A \]
\[ = 0.3 \text{ A/W} \times 100 \times 1.6 \times 10^{-7} \text{ W/cm}^2 \times 100 \mu \text{m}^2 \]
\[ \approx 10 \text{ pA}. \]

While it is possible to measure such a low photocurrent, it is difficult to precisely measure photocurrents of the same order from a two-dimensional array for a large number of points at a video rate.

2.4.1 Potential change in accumulation mode

The junction capacitance of a pn-junction PD \( C_{PD} \) is expressed as

\[ C_{PD}(V) = \frac{\varepsilon_0 \varepsilon_{Si} W}{W}, \quad (2.36) \]

which is dependent on the applied voltage \( V \) through the dependence of the depletion width \( W \) on \( V \), as

\[ W = K(V + V_{bi})^{m_j}, \quad (2.37) \]

where \( K \) is a constant, \( V_{bi} \) is the built-in potential of the pn junction, and \( m_j \) is a parameter dependent on the junction shape: \( m_j = 1/2 \) for a step junction and \( m_j = 1/3 \) for a linear junction.

The following will hold for \( C_{PD}(V) \):

\[ C_{PD}(V) \frac{dV}{dt} + I_{ph} + I_d = 0, \quad (2.38) \]

where \( I_d \) is the dark current of the PD. Using Eqs. 2.36 and 2.37, Eq. 2.38 gives

\[ V(t) = (V_0 + V_{bi}) \left[ 1 - \frac{(I_{ph} + I_d)(1 - m_j)}{C_0(V_0 + V_{bi})} t \right]^{1/m_j} - V_{bi}, \quad (2.39) \]

where \( V_0 \) and \( C_0 \) are the initial values of the voltage and capacitance in the PD, respectively. This result shows that the voltage of the PD decreases almost linearly. Usually, the PD voltage is approximately described as decreasing linearly. Figure 2.14 shows the voltage drop of a PD as a function of time. Figure 2.14 confirms that \( V_{PD} \) almost linearly decreases as time increases. Thus, light intensity can be estimated by measuring the voltage drop of the PD at a fixed time, usually at a video rate of \( 1/30 \text{ sec} \).

2.4.2 Potential description

The potential description is frequently used for CMOS image sensors and hence it is an important concept. Figure 2.15 illustrates the concept [111]. In the figure,
Figure 2.14
Voltage drop of a PD as a function of time.

A MOSFET is depicted as an example; the source acts as a PD and the drain is connected to $V_{dd}$. The impurity density in the source is smaller than that in the drain. The gate is off-state, or in the subthreshold region.

Figure 2.15(b) shows the potential profile along the horizontal distance, showing the conduction band edge near the surface or surface potential. In addition, the electron density at each area shown in Fig. 2.15 (c) is superimposed on the potential profile of (b); hence it is easy to see the carrier density profile, as shown in (d). The baseline of the carrier density profile sits at the bottom of the potential profile, so that the carrier density increases in the downward direction. It is noted that the potential profile or Fermi level can be determined by the carrier density; when carriers are generated by input light and accumulate in the depletion region, the potential depth changes through the change in the carrier density. However, under ordinary conditions for image sensors, the surface potential increases in proportion to the accumulated charge.

Figure 2.16 shows the potential description of a PD, which is floated electrically. This is the same situation as in the previous section, Sec. 2.4.1. In the figure, the photo-generated carriers accumulate in the depletion region of the PD. The potential well $V_b$ is produced by the built-in potential $V_{bi}$ plus the bias voltage $V_j$. Figure 2.16 (b) illustrates the accumulated state when the photo-generated carriers collect in the potential well. The accumulated charges change the potential depth from $V_b$ to $V_q$. 
FIGURE 2.15
Illustration of potential description. An n-MOSFET structure is shown in (a), where the source is a PD and the drain is biased at $V_{dd}$. The gate of the MOSFET is off-state. The conduction band edge profile along X–Y in (a) is shown in (b). The horizontal axis shows the position corresponding to the position in (a) and the vertical axis shows the electron energy. The $V = 0$ and $V = V_{dd}$ levels are shown in the figure. The electron density is shown in (c) and (d) is the potential description, which is the superimposing of (a) and (c). Drawn after [111].

The amount of the change $V_b - V_q$ is approximately proportional to the product of the input light intensity and the accumulation time, as mentioned in the previous section, Sec. 2.4.1.

2.4.3 Behavior of photo-generated carriers in PD

As explained in Sec. 2.3.1.2, incident photons penetrate into the semiconductor according to their energy or wavelength; photons with smaller energy or longer wavelength penetrate deep into the semiconductor, while photons with larger energy or shorter wavelength are absorbed near the surface. The photons absorbed in the depletion region are swept immediately by the electric field and accumulate in the potential well, as shown in Fig. 2.17. In Fig. 2.17, light of three colors, red, green, and blue, are incident on the PD. As shown in Fig. 2.17(a), the three lights reach differ-
ent depths; the red light penetrates most deeply and reaches the p-substrate region, where it produces minority carrier electrons. In the p-type substrate region, there is little electric field, so that the photo-generated carriers only move by diffusion, as shown in Fig. 2.17(b). While some of the photo-generated carriers are recombined in this region and do not contribute to the signal charge, others arrive at the edge of the depletion region and accumulate in the potential well, contributing to the signal charge. The extent of the contribution depends on the diffusion length of the carriers produced in the p-substrate, electrons in this case. The diffusion length has been discussed in Sec. 2.2.2. It is noted that the diffusion length in the low impurity concentration region is large and thus carriers can travel a long distance. Consequently, the blue, green, and some portion of the red light contribute to the signal charge in this case.

This case, however, ignores the surface/interface states, which act as killers for carriers. Such states produce deep levels in the middle of the bandgap; carriers around the states are easily trapped in the levels. The lifetime in the states is generally long and trapped carriers are finally recombined there. Such trapped carriers do not contribute to the signal charge. Blue light suffers from this effect and thus has a smaller quantum efficiency than longer wavelengths.

**Pinned photodiode** To alleviate the degradation of the quantum efficiency for shorter wavelengths, the pinned photodiode (PPD) or the buried photodiode (BPD) has been developed. Historically, the PPD was first developed for CCDs [112, 113],
and from the late 1990s it was adopted to CMOS image sensors [40, 114–116]. The structure of the PPD is shown in Fig. 2.19. The topmost surface of the PD has a thin $p^+$ layer, and thus the PD itself appears to be buried under the surface. This topmost $p^+$ thin layer acts to fix the Fermi level near the surface, which is the origin of the name “pinned photodiode.” The $p^+$ layer has the same potential as the $p$-substrate and thus the potential profile at the surface is strongly bent so that the accumulation region is separated from the surface where the trapped states are located. In this case, the Fermi level is pinned or the potential near surface is pinned.

Eventually, the photo-generated carriers at shorter wavelengths are quickly swept to the accumulation region by the bent potential profile near the surface and contribute to the signal charge. The PPD structure has two further merits. First, the PPD has less dark current than a conventional PD, because the surface $p^+$ layer masks the traps which are one of the main sources of dark current. Second, the large bent potential profile produces an accumulation region with complete depletion, which is important for 4-Tr type active pixel sensors discussed in Sec. 2.5.3. To achieve complete depletion requires not only the surface thin $p^+$ layer but also an elaborate design of the potential profile by precise fabrication process control. Recently, PPDs have been used for CMOS image sensors with high sensitivity.
FIGURE 2.18
Behavior of photo-generated carriers in a PD with surface traps.

FIGURE 2.19
Behavior of photo-generated carriers in a surface $p^+$-layer PD or a pinned photodiode (PPD).
2.5 Basic pixel structures

In this section, basic pixel structures are described in detail. Historically, passive pixel sensors (PPS) were developed first, then active pixel sensors (APS) were developed to improve image quality. An APS has three transistors in a pixel, while a PPS has only one transistor. To achieve further improvement, an advanced APS that has four transistors in a pixel, the so-called 4T-APS, has been developed. The 4-Tr APS has greatly improved image quality, but it has a very complex fabrication process. The usefulness of the 4-Tr APS is currently being debated.

2.5.1 Passive pixel sensor

PPS is a name coined to distinguish such sensors from APS, which is described in the next section. The first commercially available MOS sensor was a PPS [22, 24], but due to SNR issues, its development was halted. The structure of a PPS is very simple: a pixel is composed of a PD and a switching transistor, as shown in Fig. 2.20(a). It is similar to dynamic random access memory (DRAM).

Because of its simple structure, a PPS has a large fill factor (FF), the ratio of the PD area to the pixel area. A large FF is preferable for an image sensor. However, the output signal degrades easily. Switching noise is a crucial issue. In the first stage of PPS development, the accumulated signal charge was read as the current through the horizontal output line and then converted to a voltage through a resistance [22, 24] or a transimpedance amplifier [25]. This scheme has the following disadvantages:

- **Large smear**
  Smear is a ghost signal appearing as vertical stripes without any signal. A CCD can reduce smear. In a PPS, smear can occur when the signal charges are transferred into the column signal line. The long horizontal period (1H period, usually 64 μs) causes this smear.

- **Large $k_BT$C noise**
  $k_BT$C noise is thermal noise (discussed in detail in Sec. 2.7.1.2); specifically, the noise power of a charge is expressed as $k_BT C$, where $C$ is the sampling capacitance. A PPS has a large sampling capacitance of $C_c$ in the column signal line and hence large noise is inevitable.

- **Large column FPN**
  As the capacitance of the column output line $C_c$ is large, a column switching transistor is required for a large driving capacity, and thus the gate size is large. This causes a large overlap gate capacitance $C_{gd}$, as shown in Fig. 2.20(a), which produces large switching noise, producing column FPN.

To address these problems, the transversal signal line (TSL) method was developed [117]. Figure 2.21 shows the concept of TSL. In the TSL structure, a column select...
FIGURE 2.20
Basic pixel circuits of a PPS with two readout schemes. $C_{PD}$ is a pn-junction capacitance in the PD and $C_H$ is a stray capacitor associated with the vertical output line. In circuit (a), an off-chip amplifier is used to convert the charge signal to a voltage signal, while in circuit (b), on-chip charge amplifiers are integrated in the column so that the signal charge can be read out almost completely.

transistor is employed in each pixel. As shown in Fig. 2.21(b), signal charges are selected in every vertical period, which are much shorter than the horizontal period. This drastically reduces smear. In addition, a column select transistor $M_{CSEL}$ required a small sampling capacitor $C_{PD}$, rather then the large capacitor $C_C$ required for a standard PPS. Thus $k_BT C$ noise is reduced. Finally, the gate size $M_{CSEL}$ can be reduced so that little switching noise occurs in this configuration. The TSL structure has also been applied to the 3T-APS in order to reduce column FPN [118].

In addition, a charge amplifier on a chip with a MOS imager in place of a resistor has been reported [119]. This configuration is effective only for a small number of pixels.

Currently, a charge amplifier placed in each column is used to completely extract the signal charge and convert it into a voltage, as shown in Fig. 2.20 (b). Although this configuration increases the performance, it is difficult to sense small signal charges due to the large stray capacitance of the horizontal output line or column output line $C_C$. The voltage at the column output line $V_{out}$ is given by

$$V_{out} = Q_{PD} \frac{C_C}{C_{PD} + C_{C} C_F}$$

(2.40)
where $Q_{pd}$ is the signal charge accumulated at the PD and $C_{pd}$ is the capacitance of the PD.

The charge amplifier is required to precisely convert a small charge. Present CMOS technology can integrate such charge amplifiers in each column, and thus the SNR can be improved [120]. It is noted that this configuration consumes a large amount of power.

### 2.5.2 Active pixel sensor, 3T-APS

The APS is named after its active element which amplifies the signal in each pixel, as shown in Fig. 2.22. This pixel configuration is called 3T-APS, compared with 4T-APS, which is described in the next section. An additional transistor $M_{SF}$ acts as a source follower, and thus the output voltage follows the PD voltage. The signal is transferred to a horizontal output line through a select transistor $M_{SEL}$. Introducing amplification at a pixel, the APS improves image quality compared with the PPS. While a PPS directly transfers the accumulated signal charges to the outside of a pixel, an APS converts the accumulated signal charges to a potential in the gate. In this configuration, the voltage gain is less than one, while the charge gain is determined by the ratio of the accumulation node charge $C_{pd}$ to a sample and the hold node charge $C_{SH}$.
The operation of an APS is as follows. First, the reset transistor $M_{RS}$ is turned on. Then the PD is reset to the value $V_{dd} - V_{th}$, where $V_{th}$ is the threshold voltage of transistor $M_{RS}$ (see Fig. 2.22(c)). Next, $M_{RS}$ is turned off and the PD is electrically floated (Fig. 2.22(d)). When light is incident, the photo-generated carriers accumulate in the PD junction capacitance $C_{PD}$ (Fig. 2.22). The accumulated charge changes the potential in the PD; the voltage of the PD $V_{PD}$ decreases according to the input light intensity, as described in Sec. 2.4.1. After an accumulation time, for example, 33 msec at video rate, the select transistor $M_{SEL}$ is turned on and the output signal in the pixel is read out in the vertical output line. When the read-out process is finished, $M_{SEL}$ is turned off and $M_{RS}$ is again turned on to repeat the above process.

It is noted that the accumulated signal charge is not destroyed, which make it possible to read the signal multiple times. This is a useful characteristic for smart CMOS image sensors.

### 2.5.2.1 Issues with 3T-APS

Although the APS overcomes the disadvantage of the PPS, namely low SNR, there are several issues with the APS, as follows:

- It is difficult to suppress $k_B T C$ noise.
• The photodetection region, that is, the PD, simultaneously acts as a photoconversion region. This constrains the PD design.

Here we define the terms of full-well capacity and conversion gain. The full-well capacity is the number of charges that can be accumulated in the PD. The larger the full-well capacity, the wider the dynamic range (DR), which is defined as the ratio of the maximum output signal value $V_{\text{max}}$ to the detectable signal value $V_{\text{min}}$:

$$DR = 20 \log \frac{V_{\text{max}}}{V_{\text{min}}} \text{[dB]}.$$  \hfill (2.41)

The conversion gain is defined as the voltage change when one charge (electron or hole) is accumulated in the PD. The conversion gain is thus equal to $1/C_{PD}$.

The full-well capacity increases as the PD junction capacitance $C_{PD}$ increases, while the conversion gain, which is a measure of the increase of the PD voltage according to the amount of accumulated charge, is inversely proportional to $C_{PD}$. This implies that the full-well capacity and the conversion gain have a trade-off relationship in a 3T-APS. The 4T-APS resolves the trade-off as well as suppressing $kT/C$ noise.

2.5.3 Active pixel sensor, 4T-APS

To alleviate the issues with the 3T-APS, the 4T-APS has been developed. In a 4T-APS, the photodetection and photoconversion regions are separated. Thus, the accumulated photo-generated carriers are transferred to a floating diffusion (FD) where the carriers are converted to a voltage. One transistor is added to transfer charge accumulated in the PD to the FD, making the total number of transistors in a pixel four, and hence this pixel configuration is called 4T-APS. Figure 2.23 shows the pixel structure of the 4T-APS.

The operation procedure is as follows. First, the signal charge accumulates in the PD. It is assumed that in the initial stage, there is no accumulated charge in the PD; a condition of complete depletion is satisfied. Just before transferring the accumulated signal charge, the FD is reset by turning on the reset transistor $M_{\text{RS}}$. The reset value is read out for correlated double sampling (CDS) to turn on the select transistor $M_{\text{SEL}}$. After the reset readout is finished, the signal charge accumulated in the PD is transferred to the FD by turning on the FD with a transfer gate $M_{\text{TG}}$, following the readout of the signal by turning on $M_{\text{SEL}}$. Repeating this process, the signal charge and reset charge are read out. It is noted that the reset charge can be read out just after the signal charge readout. This timing is essential for CDS operation and can be realized by separating the charge accumulation region (PD) and the charge readout region (FD); this timing eliminates $kT/C$ noise and it cannot be achieved by the 3T-APS. By this CDS operation, the 4T-APS achieves low noise operation and thus is performance is comparable to CCDs. It is noted that in the 4T-APS the PD must be drained of charge completely in the readout process. For this, a PPD is required. A carefully designed potential profile can achieve a complete transfer of accumulated charge to the FD through the transfer gate.
2.5.3.1 Issues with 4T-APS

Although the 4T-APS is superior to the 3T-APS in its low noise level, there are some issues with the 4T-APS, as follows:

- The additional transistor reduces the FF compared with the 3T-APS.
- Image lag may occur when the accumulated signal charge is completely transferred into the FD.
- It is difficult to establish fabrication process parameters for the PPD, transfer gate, FD, reset transistor, and other units, for low noise and low image lag performance.

Figure 2.24 illustrates incomplete charge transfer in a 4T-APS. In Fig. 2.24 (a), the charges are completely transferred to the FD, while in Fig. 2.24 (b) some charge remains in the PD, causing image lag. To prevent incomplete transfer, elaborate potential profiles are required [121, 122].
2.6 Sensor peripherals

2.6.1 Addressing

In CMOS image sensors, to address each pixel, a scanner or a decoder is used. A scanner consists of a latch array or shift register array to carry data in accordance with a clock signal. When using scanners with vertical and horizontal access, the pixels are sequentially addressed. To access an arbitrary pixel, a decoder, which is a combination of logic gates, is required.

A decoder arbitrarily converts $N$ input data to $2^N$ output data using customized random logic circuits. Figure 2.25 shows a typical scanner and a decoder. Figure 2.26 presents an example of a decoder, which decodes 3-bit input data to 6 output data.

Random access An advantage of smart CMOS image sensors is random access capability, where an arbitrary pixel can be addressed at any time. The typical method to implement random access is to add one transistor to each pixel so that a pixel can be controlled with a column switch, as shown in Fig. 2.27. Row and column address decoders are also required instead of scanners, as mentioned above. It is noted that if the extra transistor is added in series with the reset transistor, as shown in Fig. 2.28, then anomalies will occur for some timings [123]. In this case, if $M_{RRS}$ is turned on, the accumulated charge in the PD is distributed between the PD capacitance $C_{PD}$ and a parasitic capacitance $C_{diff}$, which degrades the signal charge.
Multiresolution is another addressing technique for CMOS image sensors [68, 124]. Multiresolution is a method to vary the resolution in a sensor; for example, in a VGA (640 × 480-pixel) sensor, the resolution can be changed by a factor of 1/4 (320 × 240-pixel), a factor of 1/8 (160 × 120-pixel), and so on. To
quickly locate an object with a sensor, a coarse resolution is effective as the post-image processing load is low. This is effective for target tracking, robotics, etc.
FIGURE 2.29
Readout circuits using a source follower. The inset shows the output voltage $V_{out}$ dependence on the time in the readout cycle [125].

2.6.2 Readout circuits

2.6.2.1 Source follower

The voltage of a PD is read with a source follower (SF). As shown in Fig. 2.29, a follower transistor $M_{SF}$ is placed in a pixel and a current load $M_b$ is placed in each column. A select transistor $M_{SEL}$ is located between the follower and the load.

It is noted that the voltage gain $A_v$ of an SF is less than 1 and is expressed by the following:

$$A_v = \frac{1}{1 + g_{mb}/g_m}, \quad (2.42)$$

where $g_m$ and $g_{mb}$ are the transconductance and the body transconductance of $M_{SF}$, respectively [126]. The DC response of an SF is not linear over the input range. The output voltage is sampled and held in the capacitance $C_{CDS}$.

In the readout cycle using an SF, the charge and discharge processes associated with an S/H capacitor $C_{SH}$ are the same. In the charge process, $C_{SH}$ is charged with a constant voltage mode so that the rise time $t_r$ is determined by the constant voltage mode. In the discharge process, $C_{SH}$ is discharged with a constant current mode by the current source of the SF so that the fall time $t_f$ is determined by the constant current mode. The inset of Fig. 2.29 illustrates this situation. These characteristics must be evaluated when the readout speed is important [125].
2.6.2.2 Correlated double sampling

CDS is used to eliminate thermal noise generated in a reset transistor of the PD, which is $k_B T C$ noise. Several types of CDS circuitry have been reported and are reviewed in Ref. [3] in detail. Table 2.2 summarizes CDS types following the classification of Ref. [3].

<table>
<thead>
<tr>
<th>Category</th>
<th>Method</th>
<th>Feature</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column CDS 1</td>
<td>One coupling capacitor</td>
<td>Simple structure but suffers from column FPN</td>
<td>[127]</td>
</tr>
<tr>
<td>Column CDS 2</td>
<td>Two S/H capacitors</td>
<td>ibid.</td>
<td>[128]</td>
</tr>
<tr>
<td>DDS*</td>
<td>DDS following column CDS</td>
<td>Suppression of column FPN</td>
<td>[129]</td>
</tr>
<tr>
<td>Chip-level CDS</td>
<td>I–V conv. and CDS in a chip</td>
<td>Suppression of column FPN but needs fast operation</td>
<td>[116]</td>
</tr>
<tr>
<td>Column ADC</td>
<td>Single slope ADC</td>
<td>Suppression of column FPN</td>
<td>[130, 131]</td>
</tr>
<tr>
<td></td>
<td>Cyclic ADC</td>
<td>ibid.</td>
<td>[132]</td>
</tr>
</tbody>
</table>

*double delta sampling.

Figure 2.30 shows typical circuitry for CDS with an accompanying 4T-APS type pixel circuit. The basic CDS circuit consists of two sets of S/H circuits and a differential amplifier. The reset and signal level are sampled and held in the capacitances $C_R$ and $C_S$, respectively, and then the output signal is produced by differentiating the reset and signal values held in the two capacitors. The operation principle can be explained as follows with the help of the timing chart in Fig. 2.31 and with Fig. 2.30. In the signal readout phase, the select transistor $M_{SEL}$ is turned on from $t_1$ to $t_7$ when $\Phi_{SEL}$ turns on ("HI"–level). The first step is to read the reset level or $k_B T C$ noise and store it in capacitor $C_R$ just after the FD is reset at $t_2$ by setting $\Phi_{RS}$ to HI. To sample and hold the reset signal in the capacitor $C_R$, $\Phi_{RS}$ becomes HI at $t_3$. The next step is to read the signal level. After transferring the accumulated signal charge to the FD by turning on the transfer gate of $M_{TG}$ at $t_4$, the accumulated signal is sampled and held in $C_S$ by setting $\Phi_S$ to HI. Finally, the accumulated signal and the reset signal are differentiated by setting $\Phi_Y$ to HI.

Another CDS circuit is shown in Fig. 2.32 [127, 133]. In this case, the capacitor $C_1$ is used to subtract the reset signal.

2.6.3 Analog-to-digital converters

In this section, analog-to-digital converters (ADCs) for CMOS image sensors are briefly described. For sensors with a small number of pixels, such as QVGA ($230 \times 320$) and CIF ($352 \times 288$), a chip-level ADC is used [134], [135]. When the number of
pixels increases, column parallel ADCs are employed, such as a successive approximation ADC [136, 137], a single slope ADC [66, 130, 131, 138], and a cyclic ADC [132, 139]. Also, pixel-level ADCs have been reported [61, 140, 141]. The place where an ADC is employed is the same point of view in the architecture of smart CMOS image sensors, that is, pixel-level, column-level, and chip-level.
2.7 Basic sensor characteristics

In this section, some basic sensor characteristics are described. For details on measurement techniques of image sensors, please refer to Refs. [142, 143].

2.7.1 Noise

2.7.1.1 Fixed pattern noise

In an image sensor, spatially fixed variations of the output signal are of great concern for image quality. This type of noise is called fixed pattern noise (FPN). Regular variations, such as column FPN, can be perceived more easily than random variations. A variation of 0.5% of pixel FPN is an acceptable threshold value, while 0.1% of column FPN is acceptable [144]. Employing column amplifiers sometimes causes column FPN. In Ref. [144], column FPN is suppressed by randomizing the relation between the column output line and the column amplifier.

2.7.1.2 $k_BT$C noise

In a CMOS image sensor, the reset operation mainly causes thermal noise. When the accumulated charge is reset through a reset transistor, the thermal noise $4k_BT R_{on} \delta f$ is sampled in the accumulation node, where $\delta f$ is the frequency bandwidth and $R_{on}$ is the ON-resistance of the reset transistor, as shown in Fig. 2.33. The accumulation

FIGURE 2.32
An alternative circuit for CDS. Here a capacitor is used to subtract the reset signal.
node is a PD junction capacitance in a 3T-APS and an FD capacitance in a 4T-APS.

FIGURE 2.33
Equivalent circuits of $kTC$ noise. $R_{on}$ is the ON-resistance of the reset transistor and $C_{PD}$ is the accumulation capacitance, which is a PD junction capacitance for a 3T-APS and a floating diffusion capacitance for a 4T-APS, respectively.

The thermal noise is calculated to be $k_B T/C_{PD}$, which does not depend on the ON-resistance $R_{on}$ of the reset transistor. This is because larger values of $R_{on}$ increase the thermal noise voltage per unit bandwidth while they decrease the bandwidth [145], which masks the dependence of $R_{on}$ on the thermal noise voltage. We now derive this formula referring to the configuration in Fig. 2.33. The thermal noise voltage is expressed as

$$v_n = 4k_B T R_{on} \Delta f.$$  \hspace{1cm} (2.43)

As shown in Fig. 2.33, the transfer function is expressed as

$$\frac{v_{out}(s)}{v_n} = \frac{1}{R_{on} C_{PD} s + 1}, \quad s = j\omega.$$  \hspace{1cm} (2.44)

Thus, the noise is calculated as

$$\overline{v_{out}^2} = \int_0^\infty \frac{4k_B T R_{on}}{(2\pi R_{on} C f)^2 + 1} df$$

$$= \frac{k_B T}{C}.$$  \hspace{1cm} (2.45)

The noise power of the charge $q_{out}^2$ is expressed as

$$q_{out}^2 = (C v_{out})^2 = k_B T C.$$  \hspace{1cm} (2.46)

The term “kTC” noise originates from this formula. The $k_B T C$ noise can be eliminated by the CDS technique, though it can only be applied to a 4T-APS, as it is difficult to apply to a 3T-APS.
2.7.1.3 Reset method

The usual reset operation in a 3T-APS is to turn on $M_{\text{rst}}$ (shown in Fig. 2.34 (a)) by applying a voltage of $V_{dd}$ to the gate of $M_{\text{rst}}$ and to fix the voltage of the PD $V_{PD}$ at $V_{dd} - V_{th}$, where $V_{th}$ is the threshold voltage of $M_{\text{rst}}$. It is noted that in the final stage of the reset operation, $V_{PD}$ reaches $V_{dd} - V_{th}$, so that the gate–source voltage across $M_{\text{rst}}$ becomes less than $V_{th}$. This means that $M_{\text{rst}}$ enters the subthreshold region. In this state, $V_{PD}$ slowly reaches $V_{dd} - V_{th}$. This reset action is called a soft reset [146]. By employing PMOSFET with the reset transistor, this problem can be avoided, although PMOSFET consumes more area than NMOSFET because it needs an Nwell area. In contrast, in a hard reset, the applied gate voltage is larger than $V_{dd}$, and thus $M_{\text{rst}}$ is always above the threshold, so that the reset action finishes quickly. In this case, $k_BT/C$ noise occurs as previously mentioned.

A soft reset has the disadvantage of causing image lag, while it has the advantage of reducing $k_BT/C$ noise; the noise voltage is equal to $\sqrt{k_BT/2C}$ [146]. By combining a soft reset and a hard reset, $k_BT/C$ noise can be reduced and image lag suppressed, which is called a flushed reset [147], as shown in Fig. 2.34. In a flushed reset, the PD is first reset by a hard reset to flush the accumulated carriers completely. It is then reset by a soft reset to reduce $k_BT/C$ noise. A flush reset requires a switching circuit to alternate the bias voltage of the gate in the reset transistor.

![FIGURE 2.34](image_url)
(a) Reset operation in a 3T-APS and (b) a flushed reset [147].
2.7.2 Dynamic range

The dynamic range (DR) of an image sensor is defined as the ratio of the output signal range to the input signal range. DR is thus determined by two factors, the noise floor and the well charge capacity. The most of sensors have almost the same DR of around 70 dB, which is mainly determined by the well capacity of the PD. For some applications, such as in automobiles, this value of 70 dB is not sufficient; a DR of over 100 dB is required for these applications. Considerable effort to enhance DR has been made and is described in Chapter 5.

2.7.3 Speed

The speed of an APS is basically limited by the diffusion carriers. Some of the photo-generated carriers in the deep region of a substrate will finally arrive at the depletion region, acting as slow output signals. The diffusion time for electrons and holes as a function of impurity concentration is shown in Fig. 2.5. It is noted that the diffusion lengths for both holes and electrons are over a few tens of micrometers and sometimes reach a hundred micrometers, and careful treatment is needed to achieve high speed imaging. This effect greatly degrades the PD response, especially in the IR region. To alleviate this effect, some structures prevent diffusion carriers from entering the PD region.

CR time constants are another major factor limiting the speed, because the vertical output line is generally so long in smart CMOS image sensors that the associated resistance and stray capacitance are large.

It is noted that the total of the overlap capacitances of the select transistors in the pixels connected to the vertical output line is large and thus it cannot be ignored compared with the stray capacitors in the vertical output line.

2.8 Color

There are three ways to realize color in a conventional CMOS image sensor, as shown in Fig. 2.35.

They are explained as follows:

On-chip color filter type Three colored filters are directly placed on the pixels, typically red (R), green (G), and blue (B) (RGB) or CMY complementary color filters of cyan (Cy), magenta (Mg), and yellow (Ye) and green are used. The representation of CMY and RGB is as follows (W indicates white):

\[
\begin{align*}
\text{Ye} &= W - B = R + G, \\
\text{Mg} &= W - G = R + B, \\
\text{Cy} &= W - R = G + B.
\end{align*}
\] (2.47)
FIGURE 2.35
Methods to realize color in CMOS image sensors. (a) On-chip color filter. (b) Three image sensors. (c) Three light sources.

The Bayer pattern is commonly used to place the three RGB filters [148]. This type of on-chip filter is widely used in commercially available CMOS image sensors. Usually, the color filters are organic film, but inorganic color film has also been used [149]. The thickness of α-Si is controlled to produce a color response. This helps reduce the thickness of the color filters, which is important in optical crosstalk in a fine pitch pixel less than 2 μm in pitch.

Three imagers type  In the three imagers method, three CMOS image sensors without color filters are used for the R, G, and B colors. To divide the input light into three colors, two dichroic mirrors are used. This configuration realizes high-color fidelity but requires complicated optics and is expensive. It is usually used in broadcasting systems, which require high-quality images.

Three light sources type  The three light sources method uses artificial RGB light sources, with each RGB source illuminating the objects sequentially. One sensor
acquires three images for the three colors, with the three images combined to form the final image. This method is mainly used in medical endoscopes. The color fidelity is excellent but the time to acquire a whole image is longer than for the above two methods. This type of color representation is not applicable to conventional CMOS image sensors because they usually have a rolling shutter. This is discussed in Sec. 5.4.

Although color is an important characteristic for general CMOS image sensors, the implementation method is almost the same as that for smart CMOS image sensors and a detailed discussion is beyond the scope of this book. Color treatment for general CMOS image sensors is described in detail in Ref. [2]. Section 3.7.3 details selected topics on realizing colors using smart functions.

### 2.9 Pixel sharing

Some parts in a pixel for example FD, can be shared each other, so that the pixel size can be reduced [150]. Figure 2.36 shows some examples of pixel sharing schemes. The FD driving sharing technique [153] shown in Fig. 2.36(d) is used to reduce the number of transistors in a 4T-APS by one [154]. The select transistor can be eliminated by controlling the potential of the FD by changing the pixel drain voltage through the reset transistor. Recently, sensors have been reported with around 2-μm pitch pixels using pixel sharing technology [155, 156]. In Ref. [156], a zigzag placement of RGB pixels improves the configuration for pixel sharing, as shown in Fig. 2.37.
FIGURE 2.36
Pixel sharing. (a) Conventional 3T-APS. (b) Sharing of a select transistor and a
source follower transistor [151]. (c) Pixels with only a PD and transfer gate transistor
while the other elements including the FD are shared [152]. (d) As in (c) but with
the reset voltage controlled [153].

FIGURE 2.37
Pixel sharing with a zigzag placement of RGB pixels [156].
2.10 Comparison between pixel architecture

In this section, several types of pixel architecture, PPS, 3T-APS, and 4T-APS, are summarized in Table 2.3, as well as a log sensor which is detailed in Chapter 3. At present, the 4T-APS has the best performance with regard to noise characteristics and will eventually become widely used in CMOS image sensors. However, it should be noted that other systems have advantages, which provide possibilities for smart sensor functions.

<table>
<thead>
<tr>
<th></th>
<th>PPS</th>
<th>3T-APS</th>
<th>4T-APS (PD)</th>
<th>4T-APS (PG)</th>
<th>Log</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td>Depends on performance of a charge amp</td>
<td>Good</td>
<td>Good</td>
<td>Fairly good</td>
<td>Good but poor at low light level</td>
</tr>
<tr>
<td>Area consumption Noise</td>
<td>Excellent</td>
<td>Good</td>
<td>Fairly good</td>
<td>Fairly good</td>
<td>Poor</td>
</tr>
<tr>
<td>Dark current</td>
<td>Good</td>
<td>Fairly good</td>
<td>Excellent</td>
<td>Good</td>
<td>Fairly good</td>
</tr>
<tr>
<td>Image lag</td>
<td>Good</td>
<td>Good</td>
<td>Fairly good</td>
<td>Special</td>
<td>Fairly good</td>
</tr>
<tr>
<td>Process Note</td>
<td>Standard</td>
<td>Widely commercialized</td>
<td>Special</td>
<td>Very few commercialized</td>
<td>Recently commercialized</td>
</tr>
</tbody>
</table>

2.11 Comparison with CCDs

In this section, CMOS image sensors are compared with CCDs. The fabrication process technologies of CCD image sensors have been developed only for CCD image sensors themselves, while those of CMOS image sensors were originally developed for standard mixed signal processes. Although the recent development of CMOS image sensors requires dedicated fabrication process technologies, CMOS image sensors are still based on standard mixed signal processes.

There are two main differences between the architecture of CCD and CMOS sensors, the signal transferring method and the signal readout method. Figure 2.38 illustrates the structures of CCD and CMOS image sensors. A CCD transfers the
TABLE 2.4
Comparison between a CCD image sensor and a CMOS image sensor

<table>
<thead>
<tr>
<th>Item</th>
<th>CCD image sensor</th>
<th>CMOS image sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout scheme</td>
<td>One on-chip SF; limits speed</td>
<td>SF in every column; may exhibit column FPN</td>
</tr>
<tr>
<td>Simultaneity</td>
<td>Simultaneous readout of every pixel</td>
<td>Sequential reset for every row; rolling shutter</td>
</tr>
<tr>
<td>Transistor isolation</td>
<td>Reverse biased pn-junction</td>
<td>LOCOS/STI¹: may exhibit stress-induced dark currents</td>
</tr>
<tr>
<td>Thickness of gate oxide</td>
<td>Thick for complete charge transfer (&gt; 50 nm)</td>
<td>Thin for high speed transistor and low voltage power supply (&lt; 10 nm)</td>
</tr>
<tr>
<td>Gate electrode</td>
<td>Overlapped 1st &amp; 2nd poly-Si layers</td>
<td>Polycide poly-Si</td>
</tr>
<tr>
<td>Isolation layers</td>
<td>Thin for suppressing light guide</td>
<td>Thick (~ 1 μm)</td>
</tr>
<tr>
<td>Metal layer</td>
<td>Usually one</td>
<td>Over three layers</td>
</tr>
</tbody>
</table>

¹LOCOS: local oxidation of silicon, STI: shallow trench isolation.

FIGURE 2.38
Conceptual illustration of the chip structure of (a) CCD and (b) CMOS image sensors.

Signal charge to the end of the output signal line as it is and converts it into a voltage signal through an amplifier. In contrast, a CMOS image sensor converts the signal charge into a voltage signal at each pixel. The in-pixel amplification may cause FPN and thus the quality of early CMOS image sensors was worse than that of CCDs.
However, this problem has been drastically improved. In high-speed operation, the in-pixel amplification configuration gives better gain-bandwidth than a configuration with one amplifier on a chip.

In CCD image sensors, the signal charge is transferred simultaneously, which gives low noise and high power consumption. Also, this signal transfer gives the same accumulation time for every pixel at any time. In contrast, in CMOS image sensors, the signal charge is converted at each pixel and the resultant signal is read out row-by-row, so that the accumulation time is different for pixels in different rows at any time. This is referred to as a “rolling shutter.” Figure 2.39 illustrates the origin of the rolling shutter. A triangle shape object moves from left to right. In the imaging plane, the object is scanned row by row. In Fig. 2.39(a) at Time $k$ ($k = 1, 2, 3, 4, \text{ and } 5$), the sampling points are shown in Row #1–#5. The original figure (left in Fig. 2.39 (b)) is distorted in the detected image (right in Fig. 2.39 (b)), which is constructed from the corresponding points in Fig. 2.39 (a). Table 2.4 summarizes the comparison between CCD and CMOS image sensors, including these features.

FIGURE 2.39
Illustration of the origin of a rolling shutter. (a) A triangle-shape object moves from left to right. (b) The original image is distorted.