COdesign and power Management in PLaatform-based design space EXploration
Design Space Exploration

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TOTAL NUMBER OF IP BLOCKS PER SOC

- 2007: 20 IPs
- 2008: 25 IPs
- 2009: 30 IPs
- 2010: 50 IPs
- 2011: 60 IPs
- 2012: 75 IPs
- 2013: 80 IPs
- 2014: 100 IPs

NOW
Almost 70 IPs per SoC

Source: Delivering Great Audio with an SoC-Ready, IP Subsystem Solution, Henk Hamoen - Synopsys, Inc. - 2012
An IP subsystem is a set of blocks that can include **hardware and software**, and there is some level of **configurability**.
Designer’s Point of View
Design space

- Cache parameters
- Number of processors
- Data width
Design Space

Cost Functions

3

designer

Performance

Power

Area
Design space

Simulation/Syn. time

1 day

1 week

Simulation time adds up

Increases time to market and risk
Better designs are not unique. They provide trade-offs with respect to the objective functions.
Heuristic optimization

Non-exact methods (heuristics) must be used.

Ultimate Pareto frontier is hardly achievable

Heuristic Design solution

Non-exact methods (heuristics) must be used.
Tools for Design Space Exploration
Design space

DESIGN OF EXPERIMENTS (DOE)
Simulate only a fraction of the designs
RESPONSE SURFACE MODELING

Create an “intelligent model” to predict better designs
Design of experiments
IP WITH 2 PARAMETERS

FULL SEARCH
Sample all the possible combinations of parameters’ values.
FULL SEARCH
Can become quickly unfeasible.

18 MIN PER SIMULATION

OVERALL TIME

5 DAYS

400 IP DESIGNS

***Average simulation time of MPEG2 decoder (3 frame dataset) on SESC simulator in 2011. Variable number of out-of-order processors with design-time configurable, private L1 and L2 caches. Configurable issue width.
Parameter 1

(FULL) FACTORIAL
Fractionally sample uniformly and systematically each dimension of the design space

IP WITH 2 PARAMETERS
IP WITH 2 PARAMETERS

CENTRAL COMPOSITE
Sub-sample systematically the design space by focusing on median median parameter values.

Improves quadratic prediction
Sub-sample randomly the design space. Uniform or stratified sampling.
Response Surface Models
RESPONSE SURFACE MODELS
Analytical, models.
Fast prediction on candidate designs.

Data source: CPU-DB - Stanford University 2012
MULTI OBJECTIVE SYSTEM OPTIMIZER (MOST)

Provides DoEs, RSMs and optimization heuristics

IP Subsystem Design/R&D team

SYSTEM MODEL

DESIGN SPACE

XML

MOST

XML

CLI

System on Chip/ Product design team
Combining response surface with design of experiments
RESPIR has been proven to obtain better solutions with respect to NSGA and MOSA for the design space exploration of a multiprocessor IP***

**RESPIR EXPLORATION FACT SHEET**

<table>
<thead>
<tr>
<th>131K</th>
<th>IP CONFIGURATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1%</td>
<td>ERROR with respect to true Pareto frontier</td>
</tr>
<tr>
<td>30X</td>
<td>SPEED-UP with respect to full search</td>
</tr>
<tr>
<td></td>
<td>CENTRAL COMPOSITE Best in class DoE</td>
</tr>
<tr>
<td></td>
<td>NEURAL NETWORKS Best in class RSM</td>
</tr>
</tbody>
</table>

***Source: G. Palermo et al. IEEE Transactions on CAD 2009**
Correlation Based DSE
Kriging learns local and global trends in the design space by modeling the statistical correlation of points.
Consider the performance of two MPSOC IP configurations with varying number of cores and the same configuration for the other parameters.

DARKER SPOTS
Correlation decreasing with different number of processors

CORRELATION = 1

CORRELATION = 0.86
Although lower, correlation on performance is still significant on the boundaries

Average correlation measured on MPEG2 decoder (3 frame dataset) on SESC simulator in 2011. Variable number of out-of-order processors with design-time configurable, private L1 and L2 caches. Configurable issue width.
Classification of the goodness of a design

Rank = 1
Just as good as you can get

Rank = 2
Less good than Pareto

Rank = 3
Classification of the goodness of a design
EXPLOIT CORRELATION

Our kriging assumes the rank of a non-simulated IPs is correlated to known IP configurations.
All models improve accuracy when increasing training samples are used.

Kriging improves more.
Current State of Design Space Exploration in the COMPLEX Project
**TARGET USE CASE**

Body Sensor Network

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**POLITO**
- Application

**POLIMI**
- LLVM source to source optimizer

**STM**
- Processor

**POLITO**
- Memory partitioning

**EDALAB**
- Conversion to SystemC

**POLIMI**
- Design Space Exploration

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**-performance**
- Energy
- Code size
PRELIMINARY EXPLORATION OF PERFORMANCE

- **AES** -38%
- **ADPCM** 33%
- **GSM** 14%
- **EDN** 60%

**45% SPEEDUP**
Combining SWAT + GCC matters.

**SWAT Maximum Optimization level**

**GCC Maximum Optimization level**

SWAT and GCC optimization levels:
- O1
- O2
- O3

-38% -33% -14% -60%
Thank You!
OSCAR ACCURACY

By specifying a desired accuracy (threshold), the chance of achieving it depends strongly on the algorithm.