Thermal/Performance Trade-off in Network-on-Chip Architectures

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Outline

• **Introduction**
  – From single-core to multi-core
  – ITRS projections

• **Key observations**
  – The ring-based organization
  – The proposed methodology

• **Results**
  • Simulation framework

• **Future perspective**
What’s next

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• **Future perspective**
Power trend: The 2004 inflection point

- From single-core to multi-core processors

Multi-core architectures era

- Number of cores is expected to increase
  - Die area is not constant to $260\text{mm}^2$
  - Higher MPU power density
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Thermal management

• Design-time analysis and optimization
  – Provides thermal map analysis of a given scenario
  – Compile-directed optimization requires full knowledge of application
  – Do not consider dynamic operating conditions

• Run-time approaches
  – Adaptive to application requirements
  – Expensive
  – Often, requires monitor/sense/actuate

• Hybrid approach
  – Design-time suggested and run-time exploited
Temperature distribution in MPSoCs

• Questions
  – How multi-programmed workload impacts temperature profile in a 2D-mesh architecture?
  – Which is the impact of different workloads?
  – How to reduce hot-spot?

• Preliminary analysis can be carried out
  – Using simulation flows, providing temperature estimation beforehand
  – Formal models can be used to optimize temperature profile and assess validity
Temperature distribution in MPSoCs (cont’d)

- **Power consumption of different applications**
  - Low variability, due to microarchitecture design (in-order pipeline)

- **Implications**
  - Hot-spot is located at the center of the chip!

<table>
<thead>
<tr>
<th>Core #</th>
<th>Placement</th>
<th>Instructions</th>
<th>Power [W]</th>
</tr>
</thead>
<tbody>
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<td>0</td>
<td>1</td>
<td>34.6%</td>
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<td>64.4%</td>
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<td>1</td>
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</tr>
<tr>
<td>16</td>
<td>3</td>
<td>3</td>
<td>12.8%</td>
</tr>
</tbody>
</table>
Ring organization of NUCA architectures

- Tile-based architecture grouping tiles with similar thermal profiles and relative location

16-cores, 2D mesh and 2 rings

Basic idea: inner rings will receive fewer CPU time to reduce power consumption, hence temperature
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Linear formal model

- **From clock-toggling to temperature**

  \[ t_{i,j} := \sum_{d \in D} (\alpha_d \cdot r_d) \quad \forall \ (i, j) \in R \times C, \]

  - \( r_d \) is the duty-cycle for island \( d \)
  - \( \alpha_d \) is the coefficient to be determined
  - \( t_{i,j} \) is the temperature on tile \((i,j)\), determined as a linear function over all thermal islands

- **From clock-toggling to performance**

  \[ p_{i,j} = r_{f(i,j)} \quad \forall \ (i, j) \in R \times C, \]

  \[ f := (i, j) \rightarrow D, \]

  - \( P_{i,j} \) is the performance level of \((i,j)\) tile
  - \( r_{f(i,j)} \) is the duty-cycle for thermal island that owns tile \(i,j\)
  - \( f(i,j) \) is a mapping function from \(i,j\) to the thermal island
Optimization: LP formulation

- **Objective**
  - Maximize the lower tile performance (fairness)

  \[ \text{max } q \]
  \[ q \leq p_{i,j} \quad \forall \ (i, j) \in R \times C \]

- **Constraints**
  - Linear performance/duty-cycle relation

  \[ p_{i,j} = r_f(i,j) \quad \forall \ (i, j) \in R \times C, \]
  \[ f := (i, j) \to D, \]

  - Linear thermal/duty-cycle relation

  \[ t_{i,j} := \sum_{d \in D} (\alpha_d \cdot r_d) \quad \forall \ (i, j) \in R \times C, \]

  - Thermal constraints on maximum allowed temperature

  \[ t_{i,j} \leq T_{max} \quad \forall \ (i, j) \in C \times R \]

- **Variables**
  - The duty-cycle to each thermal island \( d \)

  \[ r_f(i,j) \quad \forall \ (i, j) \in R \times C, \]
  \[ f := (i, j) \to D, \]
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Experimental results

- **HANDS estimation framework**
  - Design-time analysis on application performance and thermal impact

![Diagram showing the HANDS estimation framework](image)

- GEM5 (Simulation)
- Orion2.0 (Power models)
- HotFloorgen (Floorplan)
- HotSpot (MTTF, Thermal and reliability models)

**Experimental settings**

- **Multiple benchmarks configuration**
  - Different suites WCET, SPLASH2 and MIBENCH
  - Different instruction breakdown

- **Alpha-2136 like architecture**

<table>
<thead>
<tr>
<th>Processor core</th>
<th>3GHz, in-order based on Alpha21264 core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Int-ALU</td>
<td>4 integer ALU functional units</td>
</tr>
<tr>
<td>Int-Mult/Div</td>
<td>4 integer multiply/divide functional units</td>
</tr>
<tr>
<td>FP-Mult/Div</td>
<td>4 floating-point multiply/divide functional units</td>
</tr>
<tr>
<td>L1 cache</td>
<td>64kB 2-way set assoc. split I/D, 2 cycles latency</td>
</tr>
<tr>
<td>L2 cache</td>
<td>1.75MB per bank, 8-way associative</td>
</tr>
<tr>
<td>Router</td>
<td>2-stage wormhole switched (Garnet network [1])</td>
</tr>
<tr>
<td>Topology</td>
<td>2D-mesh based on Alpha21364 network processor</td>
</tr>
<tr>
<td>Technology</td>
<td>45nm at 1.1V</td>
</tr>
</tbody>
</table>
Model validation

- Accuracy of predicted temperature
  - Very good accuracy irrespective of threshold temperature
  - Low variance, limited to 0.37K

16-cores

36-cores
Reliability improvement analysis

- Theoretical and modeled reliability analysis
  - Two major (FEOL and BEOL) fault mechanisms
    - Stress migration
      \[ MTTF_{SM} \propto |T_0 - T|^{-n} \cdot e^{\frac{E_{SM}}{kT}} \]
    - Electromigration
      \[ MTTF_{EM} \propto e^{\frac{E_{EM}}{kT}} \]

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Conclusions and future works

- **We proposed a design-time thermal/performance optimization model**
  - Targeting 2D-mesh architectures and NoCs
  - Based on linear formal model suitable for LP formulation and design-time optimization
  - The proposed model can be jointly used with existing dynamic thermal management techniques

- **Future works**
  - Adoption of the proposed methodology to NoC routers
  - Greater degree of freedom: rings are partitioned in multiple area (e.g., cores on the edges or at the corners)
Kiitos!
Any questions?

Take a tour to my web site for more info and tools for:
- Thermal/power-related reliability (HANDS)
- Run-time resource management (BBQ)
- Analysis and optimization of Sw energy (SWAT)

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Validation of the performance clock toggling relation

- We assess the linear relation using a 16-core architecture with 2 rings.
- The graph shows the quasi linear behavior of the proposed model, where theoretical (dash-line) and experimental (points) data are very close.
Validation of the thermal clock toggling relation

- We assess linear relation using 16-core architecture with 2 rings.
- We sampled a huge space domain (left figure).
- The data are distributed over a virtual plane on 3d space, following a linear function (right figure).