Design automation solutions for Europe

The latest release of the MEDEA+ electronic design automation roadmap reflects an increased focus on complete system-on-chip devices, combining analogue, digital and radio frequency circuitry on the same substrate. Such chips require use of high level languages to describe circuits at the functional level – making it possible to determine user needs precisely before costly mask-making, share existing circuit designs more effectively and provide powerful testing. As a result of this initiative, European chipmakers and system manufacturers should be able to achieve faster progress and shorten time to market, thus improving their competitiveness on the global stage and increasing employment in Europe.

Electronic design automation (EDA) is a critical tool in reducing the length of the design cycle and thus speeding the marketing of new products. Even a small delay can result in lost market share – and hence reduced profitability. The MEDEA+ roadmap is therefore an important knowledge management tool, enabling EDA resources in Europe to focus on key developments to the benefit of manufacturers and consumers.

The current third release of the roadmap focuses on specific needs, at particular points in time, and with a specific time frame 2002 to 2007, as of the beginning of 2002. It is a living document and it has to grow. It is therefore subject to regular updates and contributions by the experts via a dedicated discussion forum set up by MEDEA+.

Key objectives of the roadmap include:

- Accelerating process maturity for time to volume production of new chips by increased automation in library production and early product design;
- Formalising the dialogue between system houses and semiconductor manufacturers to speed up high quality system-on-chip (SoC) design; and
- Allowing better use of the intrinsic capabilities of silicon, even very deep sub-micron (VDSM) silicon technology, which makes it possible to design complex SoC that might have tens of millions of transistors on a single chip and run at 200 MHz or more.

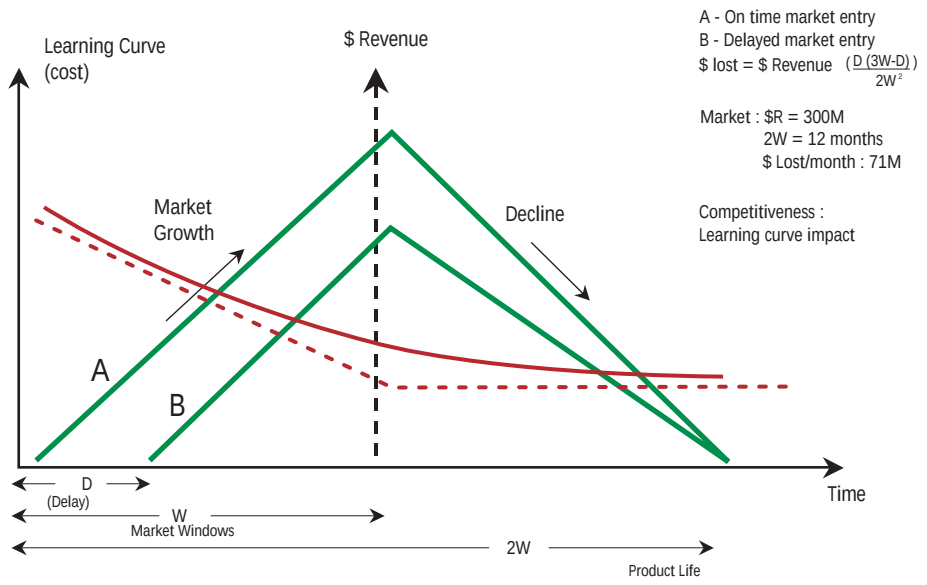
By supporting early development of processes and new products and enabling an exchange of real-time information, the roadmap will have a strategic impact on the time to market for new SoC products. As a result of this MEDEA+ initiative, the European electronics industry can achieve progress by pushing in a concerted way, ensuring major savings in resources while at the same time improving training and information exchange.

Essential to avoiding time-to-market delays

Time to volume for new electronic products has come down markedly in recent years. While it took ten years for colour televisions to reach market maturity and eight years for video recorders, the mobile phones and the latest DVD players had already reached volume levels within two years or so of their introduction.

This means that chipmakers must now develop production processes and new devices within very short periods, as time-to-market revenue penalties are high. On-time market entry also means that 100% of the market can be available – a particularly enviable situation. (figure 1)

Figure 1: The cost of time-to-market delays



Fabrication technologies are changing ever faster, with node size expected to have fallen to 5 nm by 2011, compared with 0.18 micron in 2000. The number of gates on a single device is forecast to increase from 5 to 200.10^6/cm^2 and SRAM memory capacity should grow from 60 to 240 Mbit/cm2 over the same period. This in turn implies an increase in performance from 1000 to 4000 million instructions per second (MIPS) per W.

In Europe's specialised area of application-specific integrated circuits (ASICs), the stakes are particularly high. There has been a major move in recent years from complex ASICs to complete SoC ASICs. By 2004, the number of gates in a single device is forecast to reach 100 million – compared with less than one million gates ten years before. And, over the same period, the design cycle is expected to have more than halved, from over 12 months to less than six months.

In parallel, the design methods will have changed from the bottom-up approach seen in the late 1990s, involving gate-level optimisation and a combination of different function libraries, to a genuine top-down approach with hardware-software optimisation and extensive intellectual property (IP) re-use – the target for this approach is 80% but today it stands about only 20%.

Supporting move to multifunctional SoCs

The increasing focus on SoCs makes it essential for analogue and digital designers to co-operate fully as the analogue, digital and radio-frequency (RF) elements will all be combined in a single multifunctional device. And such mixed analogue-digital circuits require effective high-level languages (HLLs) to provide overall functional level descriptions. This is a tremendous change – particularly for analogue device designers. It will require new methodologies and new generations of production processes, design tools and test equipment.

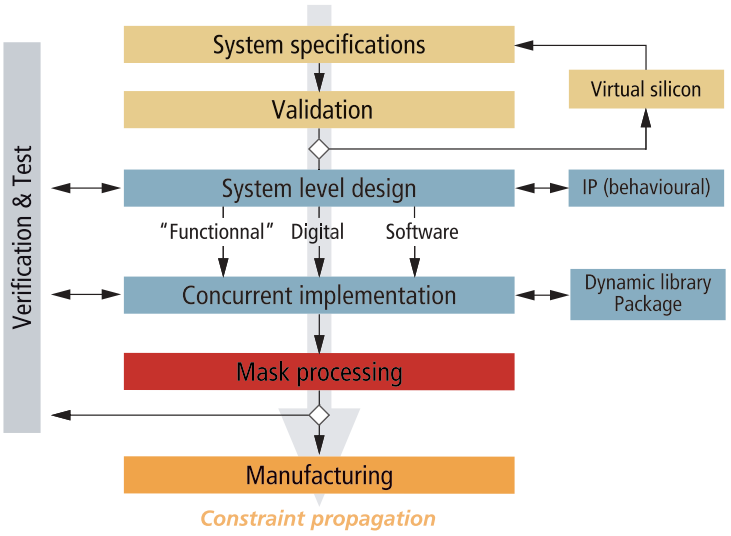
There is also a need for much better understanding of system level design. It has become essential to define systems at the functional level as it has become too complex to characterise elements at a lower level. And the complexity of these massive new chips results in problems of verification only at the chip leads. HLLs allow functional descriptions with no ambiguity – making verification possible between levels of abstraction with formal proof. This also avoids the need for simulation – some 60 to 70% of development time is currently allocated to simulation, a major cost.

Seeing what goes on inside

The problem however is bridging the gap between the technology and design automation. It is very difficult to observe what goes on inside an SoC device. In case of a device malfunction, it is necessary to go inside to find out whether it is a design or process fault. So while VDSM silicon technology offers tremendous market opportunities, it poses serious challenges to design methodology.

For example, in a 100 million gate chip, it would be necessary to check nodes, potential short circuits and excess coupling by capacitance. And faults could arise through dynamic effects. It would therefore be essential to identify the nature of the fault – with new defects arising within new technologies, such as bridges between two wires or coupling between nodes.

Figure 2: SoC targeted design flow



Such defects could be embedded deeply within the tough VDSM process. At this level, critical charges on nodes are getting smaller and smaller – in the order of 10^{-15} coulomb, which is only a few electrons. So such semiconductors react both to atmospheric radiation and to the materials being used to fabricate them: for example, boron in insulators can react to alpha particles, effectively creating mini nuclear reactions that result in charges up to 40 times the signal value – causing errors. This is a particular problem for memory cells, but non-logic devices are also affected.

The internal robustness of the chip can be improved by circuit optimisation to reduce the sensitive area of cells. A specific layer could be changed – for example the boron-containing layer. Alternatively, the results can be stored and error-correction codes (ECC) applied to compensate for such transitory errors – the stored information is replayed to replace the corrupted data.

Validating behaviour directly with user

Designing SoCs is therefore complex and specifications are very difficult, requiring a lot of work. As the mask required for the photolithographic production process can cost in excess of € 1 million, it is essential to capture users' needs exactly. This requires the type of formal description that is not yet available at general electronics industry level.

Such an approach involves the study of chip 'usage'. A virtual representation of the circuit is given to a user to try out; the user indicates any changes required and then, once overall behaviour is agreed, signs off.

This technique has already been applied in the automotive industry for future dashboard designs that incorporate features such as a camera for rear view and an electronic speedometer. Validating behaviour of the system directly with the customer has also already been used in the telecommunications industry – but not yet at SoC level, where the approach is just being introduced.

Series of detailed roadmaps

The update of the MEDEA+ EDA roadmap during 2001 and 2002 was carried out by a large number of experts (more than 50) from semiconductor companies and system houses, with much contribution from universities, public laboratories, SMEs and start-ups. The roadmap sets out to build on such new approaches to develop a series of detailed roadmaps for each step in the design process over the five years from 2002 to 2007.

Detailed roadmaps have been prepared for:

- Specification and validation;
- System architectural design;
- System to RTL HW design, system integration and RTL to gate;
- Mixed analogue/digital and RF;
- Parasitic extraction, modelling and simulation;
- IP reuse;
- Verification and validation;
- Distributed design environment;
- Low power design solutions;
- Library production solutions;
- Rapid prototyping;
- Test development for SoC; and
- Packaging.

The majority of steps are self-evident and work is well on track. However three or four points are worth emphasising:

- Removal of parasites such as alpha particles is very important due to coupling and overall noise problems as RF has to be handled on chip in SoCs and much higher clock frequencies – greater than 1 GHz – are now being used, leading to very sharp signal slopes. So signal integrity is becoming a major problem especially as RF/interconnect problems can affect the very low system voltages now being used – and voltage drops become increasingly data dependent with power consumption rising rapidly as the amount of data handled increases. All this adds another new dimension as power consumption at high frequencies was formerly affected only by the geometrical shape of the chip but now depends on data patterns as well.
- IP reuse offers a good solution in theory: a 90% reuse would give a gain of 10 in design time. But in practice, it does not always work – for example, if ten different items that were developed and tested under different conditions were then put together, it would save design time but could lead to major verification problems. As testing and debugging is often difficult at that level, reuse is not always feasible. HLL descriptions could help. The real need is for a system level design language to provide a reproducible vehicle of exchange. Europe is already leading the USA in the use of 'System C' – based on C++ class libraries – as an open source standard language for system-level design and IP modelling, and XML could provide an new 'envelope' approach that would make IP exchange more believable.
- Rapid system prototyping would operate at two levels:
  – *System level* – just to ensure the function works; and
  – *Product level* – a new step in SoC design that would provide a non-optimal chip initially with some programmability flexibility – less than 10% – in for example a single SoC for a mobile phone to capture the market earlier. The chip could then be improved (made smaller). This would offer a very cost-effective approach to design – and offer the flexibility needed in certain areas such as bank terminals, where each company would prefer some custom programmability in any case.
- Testing is always mandatory but SoCs present different dimensions. Before, testing was based on stable technologies; now technologies change every 18 months, and there is a need to design for manufacturability – the production of large numbers of devices to tough design rules could lead to costly defects and a lowering of yields. It is therefore essential to find out if a problem lies in the design or process – a big problem if there are several million gates on a chip. So, it is necessary to put more flexibility and intelligence for testing on the chip itself, particularly to help identify the wide range of transient faults that now occur. The answer is more flexible built-in self testing (BIST). As individual test algorithms in general can only handle a small range of faults, a number of BIST are now required – as well as several sorts of test data. This is particularly important when launching a new fabrication facility or ramping up production as it can have a huge impact on business. Being able to start a 'fab' for one billion devices a year one month in advance means a gain of nearly 100 million devices and can be very rewarding in terms of early capture of a market. And if good design for manufacture could boost yield by an extra 1%, this could lead to an increased output of three to six million devices over the market lifetime – providing pure profit.

Benefiting Europe and the world

The MEDEA+ EDA roadmap is a specific European initiative that has attracted much interest also from US and Asia-Pacific manufacturers. The 2002 edition is the third release – the first generation in 1999 was restricted only to participants but the latest edition has been published much more widely to the benefit of the global community. The USA has developed a more specific technology roadmap – which has become the International Technology Roadmap for Semiconductors (ITRS).

Bottlenecks still exist in the design process. When working at the SoC level and increasing IP re-use, most problems now originate in the wiring rather than the device itself. There is a particular need to resolve bus problems. This requires study of the chip layout based on interconnect and wiring constraints (coupling, parasites, ...), RF noise, DC voltage drops, short circuits and other yield problems. Future designs will therefore be much more 'wiring centric' – requiring new EDA tools by 2004, the probable date for the next edition of the MEDEA+ EDA roadmap.

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