MEDEA+ EDA Roadmap 2003

Executive Summary

I. Introduction

Over the past 30 years, the semiconductor industry has been growing so fast that "overall process" maturity has scarcely been achieved. *Process manufacturing* has been highly efficient and predictable but *design automation* lacks maturity in its engineering and performance. This is a major bottleneck, preventing the exploitation of the full possibilities of the silicon process available today (and even more in 90 nm).

The vision of the roadmap is that Design Automation can:

- **Help to accelerate process maturity for time to volume by more automation in library production, fast product design and Design for Manufacturability (DfM),**
- **Formalise the dialog between system houses and semiconductor houses for speeding up high quality systems on a chip design,**
- **Allow, even with SoC complexity in VDSM, a better use of silicon intrinsic capabilities.**

The Design Automation Roadmap, updated in 2003, gives targets that are appropriate to Europe.

Major efforts are required in five main areas:

1. Consolidation of **design automation technology** in areas such as IP (intellectual property) functions (in hardware and/or software) for greater system knowledge reuse, hardware/software co-design and deep submicron back-end and verification (60 to 70% of design time),
2. Setting up of **system-level design solutions (with the involvement of SMEs)**, including system specification, virtual and real silicon capabilities for early prototyping, usage studies and system specification validation with a 10x improvement target in design efficiency and debugging versus what is presently available,
3. Targeting **one-month design cycles** in silicon system platform solutions covering markets in which most of the software IP developments available in the platform can be reused,
4. In-depth engineering effort for **design automation solutions for manufacturability of hardware and software,** along the lines of what has already been achieved in silicon processing,
5. Early establishment of **standards** to focus development (languages, flows, single data model data base, IP's….).

A new field is becoming **strategically important,** the field of **software development** (Hardware Dependent Software and debug software), because it is becoming more resource consuming than hardware development and productivity increase of software is still at a low level (2x /5 years).

All these new constraints are pushing the development of **DESIGN PLATFORMS** (including libraries, IPs, Design Solutions, driver designs) that are **APPLICATION DRIVEN** (see ref 1: MEDEA+ Applications technology Roadmap) and allows early access to market thanks to improved top down design efficiency and reusability (see figure 1).

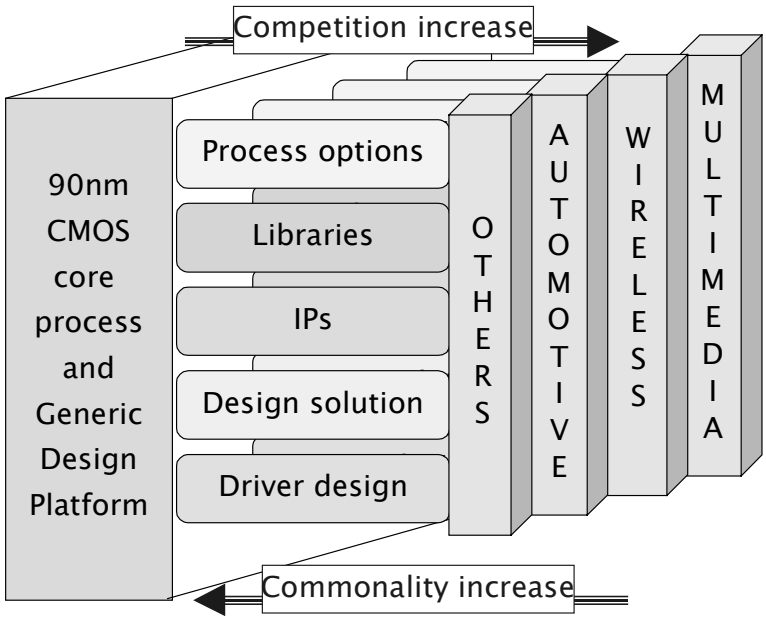

Figure 1. Example of an application technology platform

It is believed that Europe can take up such a challenge thanks to:

- A high level of maturity in silicon production,
- A deep knowledge and expertise in design automation issues, and
- An already effective collaboration between all the players (universities, national labs, R&D in companies) within Semiconductors and System Application companies.

The proposed scenario should lead – if properly staffed – to a significantly better competitive position of the European semiconductor and systems industries. It will provide the competitive advantage of higher system added value in the silicon products area in a shorter Time to Volume.

The strategic importance of early investments in Design Automation has been highlighted by a recent Ibs study [2] showing that the ranking and market values of IDM and ASICs companies are directly correlated to their EDA investments they made 5 years earlier.

An example of the correlation is given below for ASIC's, Figure 2 (10 being the highest rank).

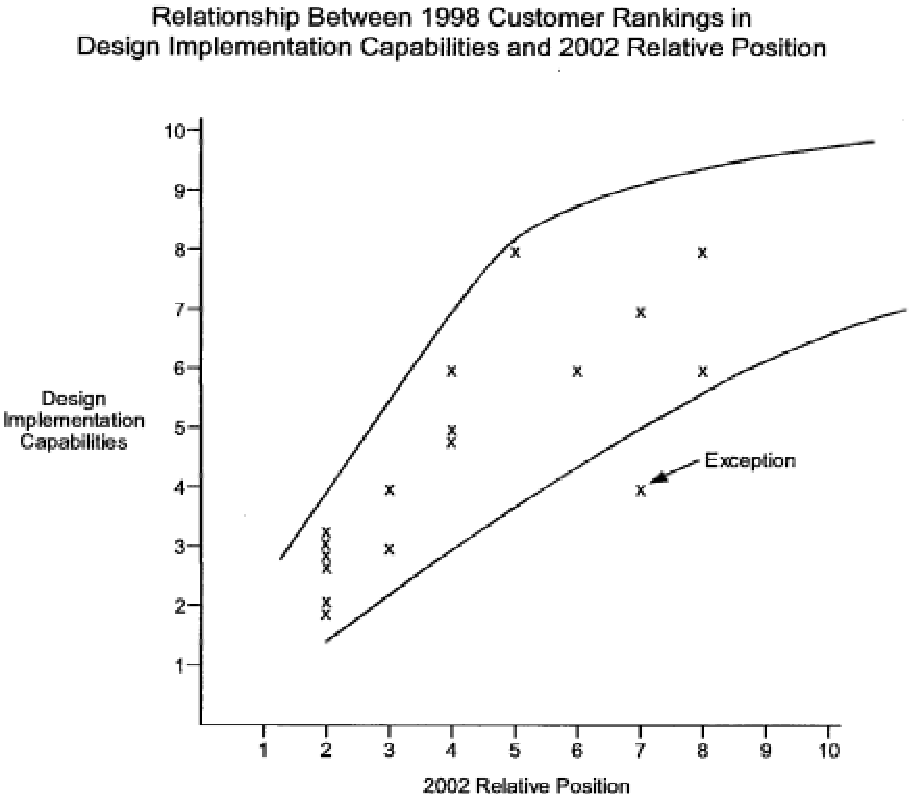

Figure 2. Asic companies ranking versus early EDA investments level.

The MEDEA+EDA Roadmap has gained worldwide attention since its first publication and today it is recognized internationally as a reference document in the domain as this is shown in the downloads of the 2002 version in the next figure (figure 3).

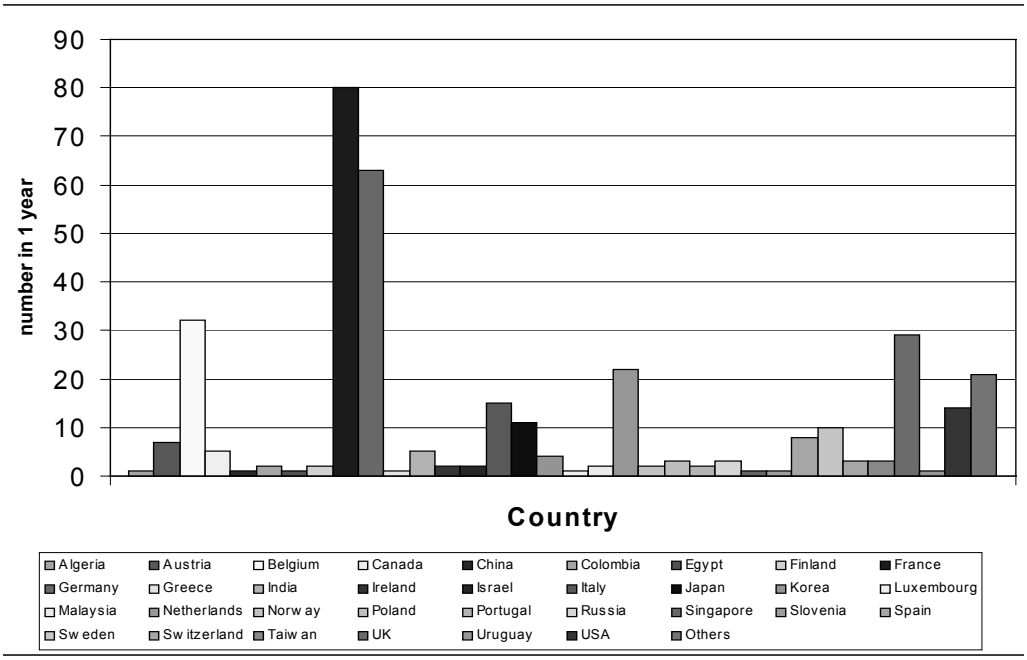

Figure 3. MEDEA+ EDEA Roadmap 2002 downloads.

Several new challenges in EDA result from the move to System on Chip capabilities with sub-100nm technologies:The huge complexities of new chips have the capabilities of complete system integration including HW and SW integration on one square centimeter of silicon, both in terms of number of active devices and of functionalities: actuators, sensors, analogue functions and RF, digital processors, dynamic, static, non-volatile memories. The rising costs of manufacturing processes and masks as well as the increasing time to market pressure are pushing to start designing with a formal and synthetisable specification system ("sign off specification"), validated with the final user to target prototypes good at the first silicon.

To Hardware development costs for new chips designs an even bigger software development cost is added: the 'Hardware Dependent Software' coming from the part of the software that is below the application layers. This development depends on the decisions and compromises made by the SoC designer (the one in charge of making the architectural decisions in the SoC design phase); see figure 4 the forecasted design costs in 90nm products.

Costs in $Million	Process	HW	SW	Total chip design	Prototype cost
1M transistors chip	.18 µm	**.18**	**.13**	.31	-
	.09 µm	**.3**	**.375**	.675	-
reference Current process capabilities	.18 µm (**20m transistors**)	**3.65**	**2.6**	6.25	.35
	.09 µm (**80m transistors**)	**24**	**30**	54	1.4

TOOLIP/MESA Workshop Grenoble 13 11 2003 Source ibs

Figure 4. Design implementation costs (0.18µm vs 90nm)

At manufacturing level, the above mentioned complexity is translated into constraints both at the design and layout levels (and their interactions) to reach high levels of yield, even for the first prototypes. This means that design and manufacturing links can no longer be ignored and should be even integrated early in the design process.

This is called 'Design for Manufacturability' (DfM). We have to move from the concept of yield to the one of "good dies per wafer" and yield is becoming strongly feature-based and no longer area-based as it used to be.

A lot of steps in the process are under the control of Design Automation tools and better interaction between process, device simulation, design and EDA tools is mandatory since the expected results involve huge savings in process ramp-up but also increased competitiveness in terms of time to market and more good dies per wafer.

II. EDA ROADMAP 2003-2006

The 2003 Roadmap covers, following the overall top down solution described earlier, the main domains where a significant amount of R&D remains to de done. It gives direction to upcoming MEDEA+ calls covering the Design Automation field.
It looks at a time window of at least 5 years in which there is a good view of what can be implemented.

In this new edition emphasis is placed:

- On system level specification validation through “USAGES”,
- On higher levels of SoC Design Platforms where a significant amount of standardisation and development remains to be done: system level design and specification (creation and validation), hardware dependent software (HDS) development in a top down design flow with a single data model data base, programmable IPs,
- On implementation levels where low power, signal integrity (crosstalk, EMC, radiation tolerance) and Design for Manufacturability (DfM) become show stoppers,
- At intermediate levels where design automation needs improvement; mixed analogue and digital, testability and repair,
- At all levels for constraint propagation, verification and test,
- At infrastructural level on concurrent engineering through distributed design data management.

The detailed 2003 roadmap document can be accessed in www.medeaplus.org.

The main topics are summarised below indicating the most relevant breakthroughs:

II.1 Linking Design Flow to Usage

SoC specifications will not be completed without the agreement of the user and this will be possible only through a virtual representation of the SoC behaviour. This implies the agreement on a behavioural formalism choice, leading to formal and partly synthesisable specifications. A link to design flow will have to be established. A virtual specification platform concept will have to be developed.

II.2 Specification and Validation

At present SoC design starts with a low level model of all parts of the system. Digital HW is described at the clock cycle level, software is present as low level code specific to a detailed architecture and finally analogue parts are given at the physical level. The global interconnect is done at the wire level which makes the early detection of bugs difficult. Higher abstraction levels for interconnecting components is the key issue to allow for SoC design . Abstraction schemes for interconnecting heterogeneous components will be required at different levels from specification to implementation.

II.3 Hardware dependent software

Hardware Dependent Software (HDS) is a new ingredient of SoC design efficiency since more resources today are needed to develop HDS than for developing hardware itself. This part of the software development, under the responsibility of the

SoC designer, is tightly linked to the architectural choices and the performances of the final product. There are several areas of improvement in HDS integration and mapping, code generation and optimisation. The final objective will be to have automatic code optimisation techniques for HDS-IP integration, optimised RTOS and communication interfaces.

II.4 System Architectural Design

Future SoC designs will accommodate complex architectures that require the exploration of a large solution space to select :

- A global communication architecture that may be bus or Network on Chip (NoC)..,
- Partitioning system specification and allocating components (IPs) to execute them,
- Deciding on local communication architectures to interconnect components to global communication architecture.

Current design approaches start with low level models of components and interconnect when most architectural decisions have been fixed. The requirement is to be able to perform architecture exploration from a higher level with constraints.

II.5 System to RTL

Integration and synthesis of hardware, software and interface components will increase design efficiency and quality. This represents a step towards a more integrated flow from specification to implementation. Particular care has to be put on transaction level modelling and platform based design.

II.6 Mixed Analogue/Digital and RF

Moving to a top-down description of this part of a SoC will be a major challenge. It requires hierarchical 'synthesis' solution to transfer a system level behavioural description to analogue building blocks or transistor level components. The global simulation and performance estimation environment needs to be developed with high flexibility and performance capabilities.

For both steps - top-down design and verification – appropriate behavioural modelling will be a key enabler. In order to manage the increasing complexity formal verification methods have to be introduced.

IP reusability will be even more important than in the digital domain but much more complicated to implement.

II.7 Parasitic Extraction, Modeling and Analysis

Due to decreased supply voltage with equal power consumption, higher clock frequencies, smaller critical charges on nodes (Qcrit.) several phenomena will cause transient faults in circuits that will require:

- Better layout and technology of power rails,
- Transient fault tolerance avoidance mechanism on chip (cross talk, ground bounce, radiation's…..) in combination with the application,
- Powerful parasitic analysis and simulation environment.

II.8 IP-Reuse Platform

IP Reuse is the only solution to speed up design productivity but still lags far behind needs. Object oriented languages, high level design views creation, analogue IP's and data base support tools are some of the breakthroughs necessary to achieve at least 90% reusability in an Application Driven Design Platform.

This will be possible through an integration-driven reuse methodology based on a platform for plug & play of efficient reuse support tools. This methodology must support the integration of IPs at different level of abstraction starting from the (functional) transaction level to the RT one, using IP modeling methodology.

Along with IPs fast and easy integration, the platform-based design will specify and provide a continuous and complete design flow methodology from Hardware/Software partitioning to RTL generation. Therefore, a platform based design methodology has to be flexible enough to be linked to any existing in-house design flow.

II.9 Verification and Validation

Verification and validation today, take more than 50% of design time. Elementary techniques both at system level (formal methods) and at architectural level (model checking, simulation, evaluation…) exist but they need to be strongly improved and linked to have a complete top down verification flow concurrent to constraints propagation.

A standard language for a link to test (test benches, test environments) needs to be defined. The final goal will be to implement, as soon as possible, the virtual prototyping concept to ease validation and verifications.

II.10 Distributed Design Environment

The large amount of data in a SoC design will require the need for a move to distributed databases that have incorporated the right trade-off between a central data-repository and scheduled synchronisation between over the net design centers working concurrently. Consequently, project management will require access to design data in the distributed design environment (IP's and other designed blocs) in highly secure conditions.

II.11 Low Power Design Solutions

The real limiting factor in SoC design today is no longer represented by integration density, as it was in the past. Instead, the hot issue to be faced with is power dissipation and power density on tomorrow's SoCs.

Some design and technology issues related to power efficiency are becoming crucial, in particular for power optimised cell-libraries, reliability issues (i.e.: IR drop, electro-migration, hot-electrons), clock-gating and clock-trees optimisation, leakage current for 90nm and below.

In the longer term, emphasis will move to architectural level (software energy optimisation), optimum memory hierarchy organisation and run time system management.

II.12 Library Production Solutions

Library creation is becoming a problem of huge database management, including the IP instances management for intra or Internet use. Security, performances and data consistency are the critical points for these databases.

Tools for schematic optimisation, auto-layout and design margin must essentially be developed further.

II.13 Rapid prototyping

Rapid Prototyping (R.P.) covers two areas:

- System R.P. to validate and debug system specifications and functionalities, an increasing need with SoC,
- Product R.P. of advanced designs for early capture of a market and production ramp up start.

In both cases, the availability of IPs (HW and SW) and reconfigurable methodologies and technologies are necessary.

II .14 Test development for SoC

Production and characterisation test cost are becoming a very significant part of final product cost (could be up to 80% in the age of Gbit DRAMS) Accordingly, a lot of effort should be invested in new testing methods allowing faster design for testability (DFT), design for debug (DFD) and design for repairs (DFR).

Reconfigurable BIST for memories is a short-term need for efficient fault debugging. This must be complemented at mid-term by Low-cost Core Testing featuring a methodology optimising core-level test reuse, on-chip DfT and low-cost testers. In the long term, Design-for-Debug architectures and tools will allow fast localisation of flaws in multi-million transistor SoCs.

II.15 Design for Manufacturability

Ramp-up of new fabs and cost of manufacturing of sub-100nm products are becoming strategic factors for competitiveness: Time To Market and the capture of new markets will directly depend on how fast new fabs will be available for production and how many good dies per wafer will be obtained.

Performance in this area will be directly related to how deep is the link between EDA and Manufacturing to improve such process improvements as:

- Early detections of new defects (observability of defects, new models, reparability…),
- Sorting area based from feature based defects,
- Feedback on design rules and libraries to maximise the number of good dies per wafer.

III. CONCLUSION

The roadmap described in this document is part of the overall development effort of MEDEA+ to reach an adequate design efficiency and maturity to handle **all the design steps** between the two extremities of the design process:

- System Level Design and,
- Signal Integrity Solutions.

This needs to be understood in an increasingly competitive environment due to SoC specifics (**platform based design, IPs…)**.

It also underlines the increasing role of **Hardware Dependent Software** (without immediate achievable solutions for a significant productivity increase) which is requiring similar amounts of resources in modern SoC design as is Hardware.

In conclusion, a significant amount of work remains to be done in **Design Platforms** such as:

- Virtual prototyping and system validation,
- Top down design methodologies (with constraint propagation, verification and test capabilities),
- Analogue, mixed, RF and MEMs,
- Hierarchical IP reuse (both HW and SW) with a complete standardisation of the languages,
- Very Low power design and Signal integrity solutions for V.D.S.M. (including Transient Fault Tolerance).

The move to sub-100nm critical dimensions pushes EDA, Process and Design to work more closely (Figure 5) to achieve better market performances.

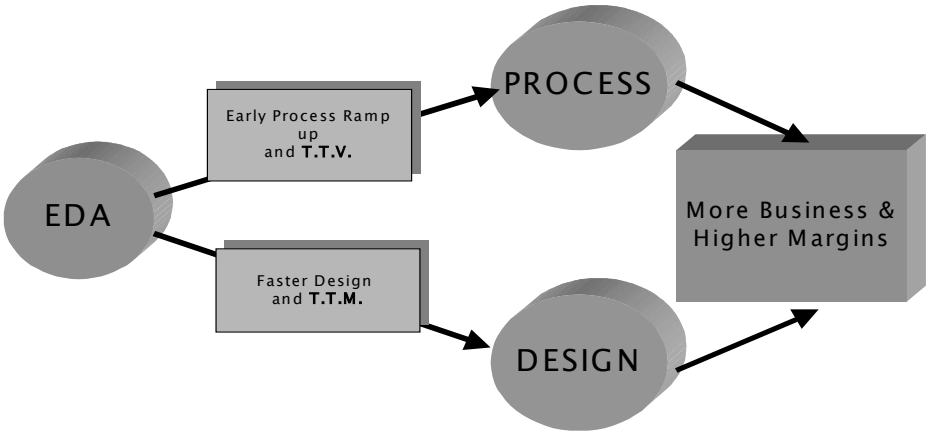

Figure 5. EDA as an 'enabler' for process and design

This will be around a **common data base** for sake of real time interactivity between design, libraries, process, design rules…This is the only way to reach a global optimisation of the solution for the system customer (new process development, fast production ramp up, prototypes good at the first run).

European **EDA start-up's and SME's** also need a dedicated support to move together to a **single SoC design solution** environment offering, rather than staying at point tools level offering which cannot compete on a world-wide basis. This will contribute also to the adoption of Standards and more engineered solutions in Design Automation.

The involvement of the European companies in the MEDEA+ Roadmap continues to be very strong. This is a good trend that must be pursued (in particular the semiconductor houses mostly through Philips, Infineon and ST but also the system houses mainly through Alcatel, Bull, Thales, Italtel, Bosch, Fiat, Siemens and with numerous contributions from Universities, national laboratories, SME's and start-up's).

One of the activities to be improved remains the EDA Forum where we need to reach a permanent level of dialog and exchanges to create the European EDA community. It should also be an environment to share information and statements on a permanent basis. This must be the major effort from now on.

Last but not least, this work would not have been possible without the constant encouragement of the MEDEA+ management team as well as the support of all the MEDEA+ Office personnel.

References:

[1]-MEDEA+ Design Automation Conference Nov.04-06, 2003, Stuttgart.

"Roadmapping in MEDEA+"

[2]-Same conference.

"Strategic dependence of business in VDSM technologies on Design Automation".

Hendel Jones: International Business Strategies.

[3]- EDA roadmap and Applications technology roadmap web sites:

visit http://www.medeaplus.org, section 'Publications'