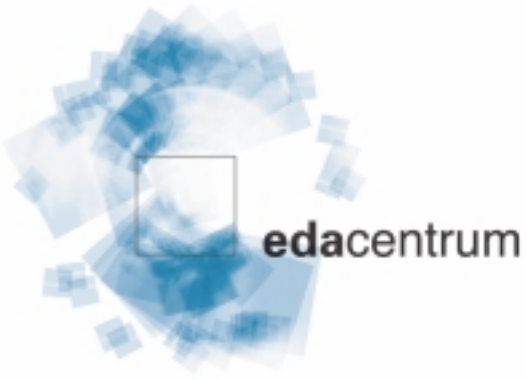
EDA DESIGN AUTOMATION ROADMAP

EXECUTIVE SUMMARY



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FOREWORD

Under the guidance of MEDEA+ Applications Steering Group a Design Automation Roadmap for future requirements for the European Industry has been released in March 2002.

The edacentrum and the MEDEA+ Office, have decided to commonly publish an Executive Summary of the MEDEA+ 2002 EDA Roadmap, bearing in mind that Top Management in Industry, Academia and Public Authorities are rather preferring to get acquainted with this specific topic in a more comprehensive document.

Those who prefer reading the more detailed version are recommended to download the Roadmap from http://www.medeaplus.org/webpublic/publ_relation_eda.htm.

Under the same address you will find an EDA Roadmap Discussion Platform, accessible to partners and co-operative companies, where experts of the Electronic Design Automation are exchanging opinions and sharing views on a regular basis.

May we give our sincere thanks to all those who supported the publication of this Executive Summary of the MEDEA+ 2002 EDA Roadmap.

MEDEA+ Office **edacentrum**

February 2003

Introduction

Publication of the third edition of the MEDEA+ Electronic Design Automation (EDA) Roadmap highlights the growing importance of complete system-on-chip (SoC) solutions, combining analogue, digital and radio frequency circuitry on the same substrate. Very deep submicron devices (VDSM) are essential to meet the demands for increasing miniaturization, higher levels of integration, and system innovation for low cost electronic applications.

Today current 0.18 um silicon technology enables SoCs with up to 5.10^6 gates/cm^2 and is capable of handling up to 1000 million instructions a second (MIPS) per Watt with clock frequencies up to 720 MHz. Already by 2004, 90 nm technology should make possible 30.10^6 gates/cm^2, handling up to 2200 MIPS/W and clock frequencies up to 1300 MHz. And by 2011, 50 nm technology will make it possible to have SoCs with 200.10^6 gates/cm^2, handling 4000 MIPS/W and clock frequencies up to 2 GHz.

Such a complex SoC development requires management of the total value chain, from initial design to manufacturing in volume at the lowest possible cost. Though industry process manufacturing is highly efficient and predictable, design automation still lacks maturity in its engineering and performance and is thus preventing exploitation of the full possibilities of the silicon process available today. The vision of the roadmap is therefore that design automation can

- help to accelerate process maturity for time to volume by more automation in library production and early product design,
- formalize the dialog between system houses and semiconductor houses for speeding up high quality systems on a chip design, and
- allow, even with SoC complexity in VDSM, a better use of silicon intrinsic capabilities.

Applications for these new circuits will include sophisticated automotive control systems for safer and more energy-efficient cars, high-performance yet easy-to-use consumer electronics and versatile, yet secure, mobile Internet multimedia terminals offering a much higher quality of service with a choice of connectivity (VDSL, wireless, optical…) and able to handle services such as video on demand. These devices will offer a high level of functional intelligence – improving man-machine interfaces, automating translations and simplifying communications.

The MEDEA+ roadmap is therefore an important knowledge management tool, enabling EDA resources in Europe to focus on key developments to the benefit of both manufacturers and consumers. It highlights specific European needs from 2002 to 2007, as seen from early 2002, and provides a series of detailed roadmaps for each step in the design process, identifying the requirements and obstacles. Figure 1 provides an overview on various domains covered in the 2002 Roadmap.

Fig. 1: Detailed Roadmaps by domain

- Specification and Validation
- Distributed Design Environment
- System Architectural Design
- Low Power Design Solutions
- System to Gate
- Library Production Solutions
- Mixed Analogue/Digital and RF
- Rapid System Prototyping
- Parasitic Extration, Modelling and Simulation
- Test Development for SoC
- Packaging
- IP Reuse
- Verification and Validation

Over 100 experts from semiconductor companies and system houses have contributed to the development of the EDA roadmap during 2001 and 2002, with additional input from universities, public laboratories, SMEs and start-up companies. MEDEA+ and edacentrum feel obliged to express their sincere appreciation to all these experts.

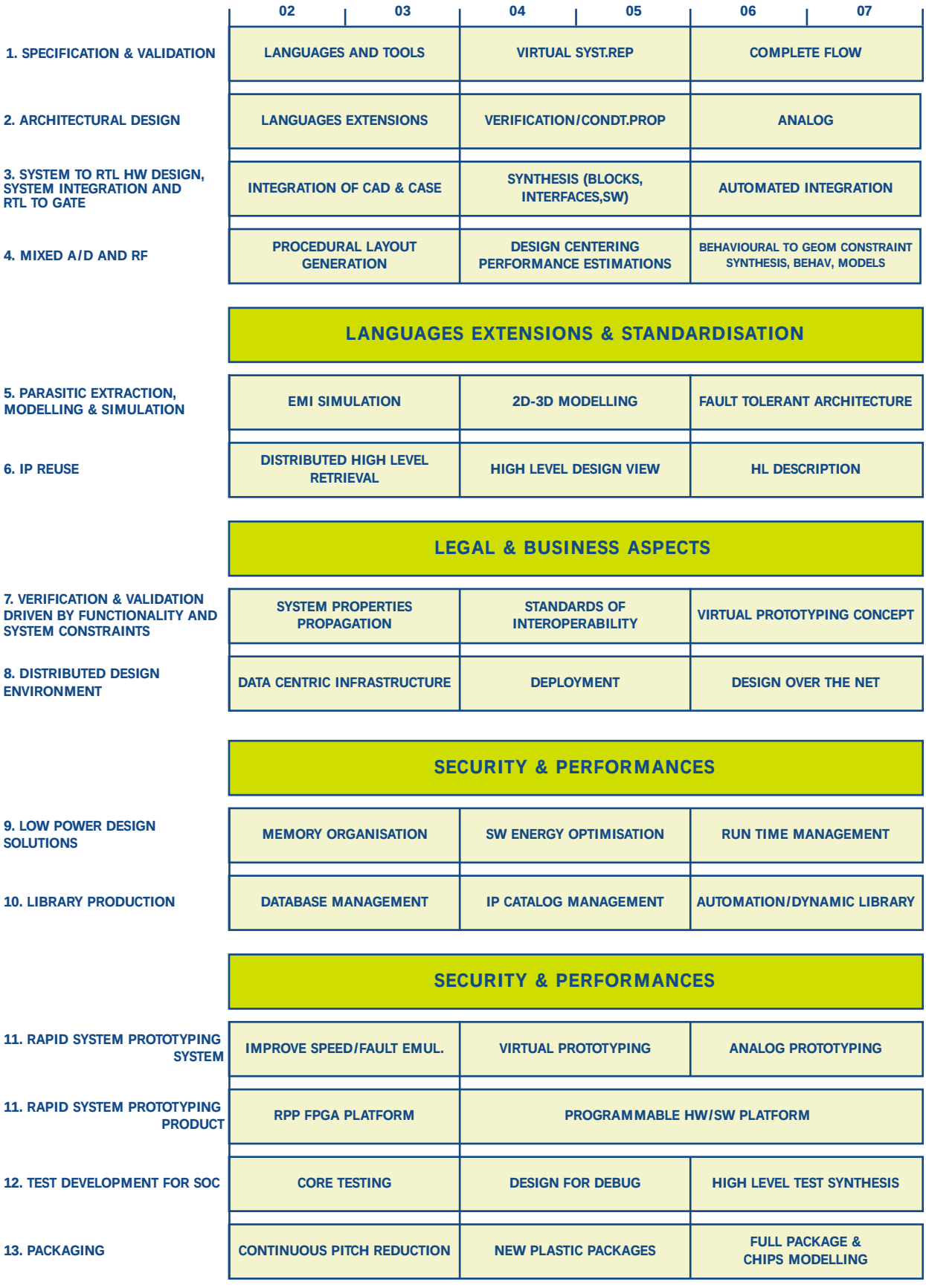
It is clear that there is still significant work to be done in line with the future application platforms, such as:

- Virtual prototyping and system validation
- Top down design methodologies (with constraint propagation, verification and test capabilities)
- Analog, mixed and MEMs
- Hierarchical IP reuse (both HW and SW) with a complete standardisation of the languages
- Signal integrity solutions for VDSM (including Transient Fault Tolerance)

The roadmap will of course continue to be updated regularly with contributions from the experts through a dedicated discussion forum set up by MEDEA+.

Figure 2 gives a more detailed content of the EDA roadmap.

Fig. 2: SoC Mixed Analogue/Digital Design and Test Roadmap (Global Breakthroughs)



1. Specification and validation

In DSM (deep submicron) processes, ever-increasing chip complexities have led us to the point that more than 50% of the first silicon do not meet specifications. There is an urgent need to establish formal specifications that can be validated between consumer and supplier through virtual silicon.

At present, several system specification languages exist, but they require huge descriptions for complex systems, they are not suitable for groups having different cultures and expertise, and most of them cannot be combined. What is needed are multi-language methods – either a set of standard languages (such as VHDL and Verilog HDL) or one multi-paradigm language integrating libraries with various paradigms. Multi-language methods imply a need for inter-operability between languages – e.g. a specification in a given language that makes use of subsystems described in "foreign" languages.

The effective use of a given specification language requires the availability of computer-aided methods. Current EDA frameworks are difficult to scale for handling and managing millions of lines of code models. Modern software engineering technologies need to be introduced to integrate large database management and to allow for co-operative Internet development. In the longer term, support of geographically distributed teams working on a central database is required.

A huge gap exists between specification and implementation; few high-level methods give a link between already existing tools and an EDA (Electronic Design Automation) environment. The ultimate goal would be to employ formal methods to prove the validity of the refinements performed on the initial specification and to develop testbenches.

For further support of multi-paradigm languages and modern EDA frameworks, high quality libraries are a vital need. They make it possible to customize a given tool, language or environment for a specific application domain or technology.

2. System Architecture Exploration and Partitioning

One of the most frequent tasks in architectural design is that of partitioning in order to deal with the high complexity of a given design. Methodologies and tools are well established on RT level and below, but not on higher levels. For higher levels including transaction-level communication, it requires new specification mechanisms and constraint budgeting will have to seamlessly connect to existing low-level constraint methodologies. Mixed-signal designs will also have to be investigated.

Performance evaluation is the backbone of architecture analysis and exploration. Today, it is restricted to the estimation of speed. Research work is needed for specifying performance criteria and estimation. The design cycle has to be made more efficient and shorter by developing seamlessly linked performance estimation methodologies and tools. As a next step analogue subsystems have also to be covered.

Hardware/software partitioning will be application specific in order to cover SoC product design efficiently and has to take into account restricted platforms. Hardware/software partitioning has to handle multiprocessor architectures with a complex memory architecture, automation of the iterative exploration of solutions is required as well as support of analog/digital partitioning.

As IPs made of complex cores has complex specifications and sophisticated interfaces, tools are needed for performance estimation and selection of IP. Different standards for specification and interfaces as well as trade-offs between performance and business issues have to be addressed by the selection process.

Transaction-level communication has to be translated into a series of transactions involving a number of sub-problems as interface synthesis and selection of a communication structure. Interface synthesis is needed at higher levels of abstraction, including implementation level, driver level and application level as well as digital/analogue interfaces. A controllable and predictable methodology for efficient implementation of complex communication structures is required.

Algorithm selection is important to make effective use of on-chip computation, communication and memory resources. Algorithm selection and optimisation is closely related to availability of performance estimation techniques. Designers will need a well-defined methodology to optimise various aspects of an algorithm by transformation, even if it is unlikely to be a fully automated methodology.

Linking architectural analyses and hardware/software co-design to a design flow should produce a tremendous increase in productivity and system optimisation. With a complete design flow including implementation and hardware/software co-design, architectural exploration will become easier. The definition of a reference design flow still needs lots of research. The design of SoC products would also require linking digital and analog design flows together.

3. System to RTL Hardware Design, System Integration and RTL to Gate

Hardware/software co-design needs to assess the expected delays, the area needed and the performance in an early state of design and as precisely as possible. Standard components, IP cores and behavioural synthesized modules are more and more often integrated into SoCs. This implies the need of generic template descriptions and the aspect of validation, in particular new and efficient debugging methods of hardware and software with its interfaces. The usage of IP cores and the sophisticated memory structure require a continuous integration of the involved synthesis tools at all levels of abstraction. The design of multi-million gate ASICs requires an extremely advanced level of expertise to achieve first time right designs. Reconfigurable hardware like FPGAs reaches new fields of application. Electrical noise induced by digital communication in the analog parts of the SoC must be estimated.

Today, behavioural synthesis tools only support VHDL or Verilog HDL as input languages and component sharing is restricted to one process while high-level languages like SystemC, C++, C, Java and SDL are used for specification. Behavioural synthesis usually has an ASIC-like target in mind. IP is often not delivered with extensive testbenches. The visibility of internal nodes at

gate level is reduced due to the actual synthesis procedure.
Short-term goals are to extend the class of input languages such as SystemC, C++, C, Java, SDL, and Matlab for behavioural synthesis. Existing tools for logic synthesis, floor planning and layout generation must be improved to provide efficient interactions among those point tools. New mechanisms and formalisms for specification of complex parameters of Software- and Hardware-IPs have to be developed.
Future trends will establish standards and automation for defining, characterizing, emulating and integrating IP cores. The synthesis of multi-process and interface descriptions must be provided to automate system integration. Distributed hardware simulation is necessary. A full integration of floor planning, synthesis and physical implementation in one iterative process from RTL to gates in a transparent manner must be established. Co-debugging of hardware and software components should be supported as well as heterogeneous emulation platforms.
Standards and tools are necessary to map specifications and architecture level IP modules. Synthesis tools should provide an instrumentation mechanism to include IP hardware descriptions. As 70% of the delay is in interconnects, it is necessary to focus on developing an accurate algorithm estimating the overall circuit delay.

4. Mixed Analog/Digital and RF

The main five topics are description languages and system exploration, circuit synthesis and sizing, schematic validation, design for manufacturing and analog/RF layout synthesis. As a major goal the need of more top-down in design methodology is obvious. This includes system level approaches (including simulation and behavioural model generation) and multi level design verification strategies as well as the harmonization of data formats and data management through all levels of abstraction. Another important aspect regarding all five topics is the integration of RF issues into the design flow.
In a mixed signal design flow, description languages and system exploration have to be improved by integration of system level design methodology, including hierarchical and reusability aspects. An automated transformation of specifications and models between system, control and electrical level has to be enabled and established among designers. This goal can be met by new specification techniques and behavioural modelling strategies that consider the necessities of mixed-signal and RF aspects. This touches topics like behavioural model generation, their transfer, their parameterisation and their reuse as well as HDLs (e.g. SystemC, VHDL and Verilog HDL), numerical methods and modes for simulation and an early consideration of physical effects. As long term goal, this will lead to a unified object oriented top down methodology, capable of parametirization and reuse for hardware/software-digital/analog and RF systems.
Circuit synthesis and sizing suffers from shrinking processes and growing complexity. Tools for topological synthesis are near a myth, except for special circuit classes with regular structure. Merely sizing and symbolic methods have become to be a matter of automation using strategies of characterization optimisation, computer algebra and computation power. These approaches are estimated to be extensible, in order to investigate different circuits and to include deep-submicron-, layout-, and RF aspects into a synthesis methodology exploiting mainly reuse. In the end, the wish for automatic synthesis is reduced to the long-term goal of analogue IP reuse, which means a reuse of design knowledge including generic parameterised topologies and hierarchical aspects.
The time consuming process of schematic validation called characterization has always been an important topic in mixed-signal design. This will change, because automatic characterization methods have been established. However, they lack generality because of their in-house character and their inhomogeneous composition of different analogue and digital tools. This leads to the demand for a standardized characterization language and a well composed collaboration of these tools, e.g. digital and analogue simulators. As long term topics, the consideration of parasitic and post layout effects and hierarchical aspects will have to be considered in characterization, as well as formal verification has to be taken as an opportunity to avoid long stimuli patterns.
Design for Manufacturing is essential in order to have first time success in shrinking processes and growing complexity. This leads to tasks like the creation of optimised safety margins, the consideration of the growing influence of local parameters and the establishment of statistical parameter extraction and model development. To reach these goals, the investigated statistical modelling and design techniques need to be extended from CMOS applications to others and have to include RF specific needs. Further on, the methodology needs to include statistical analysis in all levels of abstraction including worst case and yield and it needs to consider sizing and test. Another important long term issue is the minimization of measurements on silicon, which would speed up the time consuming analysis of process characteristics.
Analog and RF layout synthesis is far behind digital, because it exists just for “standard analogue blocks” and neither floor planning nor hierarchical capabilities have been realized yet. As short term goals, there is a strong need for

- constraint handling, which covers the whole flow,
- compaction algorithms, which are capable of analog and RF,
- a bi-directional linking between analog and digital block and
- the extension of the open generator programming environment, which at present is restricted to device level.

These goals can be met by introducing new methods on standard blocks, before they are extended to more complex blocks and hierarchy. Thinking in long terms, layout synthesis for all kinds of analogue blocks and applications as well as covering RF and different technologies including parasitic effects, electrical constraints and reuse is expected to become reality.

5. Parasitic Extraction, Modelling and Simulation

Due to increasing clock rates up to 10 GHz, high transfer rates (40 Gbit/s), decreasing power voltages and very small cross section dimensions in the entire microelectronics area (partly also in MEMs) the sensitivity to any parasitic effect because of the reduced noise margins will be important. Consequently, an increasing demand for the efficient treatment of parasitic effects in the complete design process of microelectronic systems will arise.

In the future, no distinction between time and frequency response will exist (up to 110 GHz). I.e. digital, analogue design and RF design will grow together. Due to high packing density, the different physical interferences (electrical, thermal, mechanical) have to be treated concurrently. These interferences have to be considered for all along the design flow, starting from the early design stages, while refining the modelling and the simulation accuracy.

The present and planned advances in microelectronics and MEMs will be of little benefit if the signal integrity problems will not be included in the design methods. It is absolutely necessary to combine the different design demands of the IC (on chip) and the subsystem (off chip) because packaging plays a key role in the future. Consequently, new methods for SI/EMC/RF compatible design of microelectronic systems have to be developed. To minimize SI/EMC/RF problems, appropriate design rules and models have to be considered during all design stages.

Therefore, there is a need for EM simulations in 2D and 3D within the environment of chips and the derivation of simplified macro models for use in higher-level simulations. One of the most challenging problems in ultra deep sub-micron CMOS technology is the parasitic coupling effect between on-chip interconnects. The use of specific dielectric materials (so called SiLK for Silicon Low K) to reduce the coupling capacitance will help in the near future only. There is still the need for better interconnect materials.

In the upcoming years, IC immunity to EMI will be one of the major concerns of system and integrated circuit designs with low power supply IC voltage. The problem of electronic system and IC immunity to RF and pulsed interference is extremely important in electronic applications devoted to control system safety. Signal integrity problems will continue to grow in the future. It will become necessary to think about radically new computational methods, likely based on a hierarchical splitting of the model and a selective extraction of 3D and 2D structures when appropriate, using for example boundary FE techniques.

Other problems are the timing faults due to the simultaneous occurrence of signal integrity problems and fabrication defects. Process parameter variations and various defects (shorts, opens…) often increase the delays of circuit paths. In multi-MHz circuits, even short delay variations may result in timing faults. Thus, the automatic insertion of fault tolerance and other robustness techniques will become mandatory for correct system operation as the systems become very complex and their basic components become nanometric. The requirements are to integrate the signal integrity problems and the appropriate checks in new EDA tools or design flows.

6. IP Reuse

Design reuse methodology is expected to be the key enabler in the area of design methodologies to face both short and long term development objectives. However, moving to effective design reuse methodologies will require the industry to harmonize business practices related to the exchange and qualification of virtual components (VC).

At present, basic research has been mostly finished and advanced methodologies are under investigation (e.g. classification, adaptation, verification and platform-based design), but a comprehensive tool integrated into a standard design flow is not yet available on the market. Existing hardware reuse approaches lack the possibility to support several abstract levels of description and design. The approaches available are restricted to one major or minor reuse aspect. A comprehensive methodology is missing, which combines and integrates different domains (hardware and software related features) into one common reuse approach, i.e., design strategies, testbenches, documentation, test conditions and solutions. This holds for analog as well as for digital components.

As a conclusion, several concrete research issues deserve detailed attention: quality and exchange, IP specification, customisation and parametirization, management and database, platform-based design, and legal and business aspects.

Today, the exchange of virtual components is not efficiently supported since basic quality attributes are not applied and exchange standards are poorly developed. A methodology for IP qualification is needed. Currently, two kinds of IP are available: qualified IP contained in a virtual IP library applicable in different environments and unqualified IP applicable in specific environments. However, several barriers in terms of tools, flows and methodologies exist. To overcome these barriers an IP virtual library must be installed that meets the defined quality attributes for plug and play in target designs. The IP virtual library format has to support very different component and exchange formats. IP qualification tools and IP qualification centres are required to support components exchange.

The application of IP requires an adequate description of the components designed and stored for reuse. The use of hardware description languages (HDLs), such as Verilog HDL and VHDL, is not suitable due to their semantic limitations. At present, there is a lot of consensus in using object-oriented languages. Emerging cooperation between system-level standardization and defacto standard defining bodies (e.g. VSIA, IEEE, OSCI) provide first results. However, standards for embedded system software as well as for high-level analogue/mixed-signal reuse are not yet available. Therefore, in a first step the definition and the characterization of different levels of abstraction, of functional and non-functional specification of components is necessary. Then, methodologies based on the separation between functionality and communication for design space exploration in a system need to be developed. Moreover, semi-automated ways for communication refinement from higher to lower levels of abstraction are needed.

Further, the plug and play of components requires a design for

reuse strategy to allow for the required parametirization capability. Currently, components can be described at different levels of abstraction and complex components can be derived from already existing components. However, mature methodologies are necessary to ensure that component adaptation can be performed quicker and with lower effort than designing it from scratch. Parameterizable components are especially well suited for reuse, but this poses a major challenge to the validation of components, as the simulation effort is intractable. New solutions have to be found and applied, e.g. formal verification. In a second step, the adaptation of components should be hidden from the reuser since the complexity requires many information details that are beyond the scope of the designer.

For integration a dedicated database-management is needed. Distributed databases for storing IP have to overcome pure storage mechanisms of IP or versioning. An IP life cycle model containing all required parameters should be provided. Then, each virtual component included in the database has to be maintained in order to take advantage of the reuse in different application (new version, adaptation to new constraints, user guideline, bug list etc.).

Specific applications result from the core competencies of the European industry, e.g. telecommunication, automotive and multimedia. Application-specific platforms are already available in-house but dedicated tools are under development only. In order to run platform-based designs, many requirements must be defined and standardized and also the verification concept must change. Testbenches have to be modular and synthesizable. A standard system verification environment will shorten the design time of complex systems and improve the quality. A higher level of abstraction has to be introduced to explore and partition a system, and incremental platform design must be addressed. In the future, other innovative approaches like micro mechanical environments become important for IP reuse platforms. A transfer of know-how has to take place on a methodological level.

The third party IP market is currently limited by a lack of standard business and legal practices widely accepted within the industry. Therefore, in-house strategies and IP protection mechanisms must be integrated into one comprehensive business model supporting IP reuse and incorporating the needs of designers, providers, and users. In the short term, a commonly accepted definition of the minimum information requirement for a VC to be considered “qualified” is needed. In the longer-term, organizations should offer royalty collection, tracking and auditing services like “clearing house” services offered in other marketplaces.

7. Verification and Validation

Over the last few years verification has clearly become a major concern to the semiconductor industry (more than 50% of design time), where it is now common to see verification teams of sizes equivalent to those of the design teams. Today's EDA solutions for validation and verification need drastic improvement. Different levels of abstraction and different verification objectives require different representations. At the lower levels of abstraction it is more effective and very little is available at higher levels. The cost of non-quality in IP blocks will increase significantly as these IPs get distributed for integration into systems or new IPs.

The documentation belonging to the IP will be of crucial importance. Formal methods must be extended from hardware descriptions to system level descriptions to make it possible to check system properties. System properties are to be propagated to the architecture level in order to verify the upward consistency. Final target is the validation of heterogeneous systems while model checking should be performed with different techniques.

Recently new tools have been introduced without a strong design flow integration policy. Non-exhaustive property checking on RT-level design descriptions can be performed but is limited to a fraction of the system that has favourable characteristics. A few commercial products have been introduced based on symbolic simulation.

A short term goal is to define a common measure, in terms of coverage that can be used at different levels of abstraction. Property checking with static & dynamic techniques should be used exhaustively at system level. Linking the theorems to be proven with the specified system properties is a prerequisite to the whole verification process. Virtual prototypes and a standard language for describing testbenches/test environments are needed.

Future needs are the addition of description levels on top of today's HDL levels to keep a human-manageable level of description and reach time-to-market goals for tomorrow's systems. A (single) formalism is needed that can capture system specifications in such a way to allow both simulation/emulation based and "formal" checking. In a system level environment the following issues need to be addressed in the next few years: System property checking, system simulation/emulation, architecture property and model checking, checking architecture simulation/emulation, constraint propagation and functional coverage.

The verification of descriptions featuring both control and data path will possibly require the integration of model checking and theorem proving techniques. Full implementation of virtual prototyping is needed beside harmonization and generalization for the higher level of abstraction.

Requirements for generic applications are that technologies, such as emulation, prototyping and analogue-dedicated simulation platforms, have been integrated into the verification process to allow architectural simulation and emulation. Different views suited for different purposes are needed and they must all (be guaranteed to) be equal. The constraints must be included in the embedding system and there should be a testbench that can be used throughout the whole design flow. Re-use of testbenches at different levels of abstraction is a crucial point.

8. Distributed Design Environment

The SoC mutation, through the tremendous increase of complexity is driving a deep and irreversible paradigm shift in the design methodologies and related design team working. Because SoC design projects involve distributed design know-how and teams dispersed geographically, the design environ-

ment infrastructure itself needs to be distributed.
The mere size of future design databases presents a limiting factor in the way design development needs to be approached. The shift from 0.18 µm to 0.05 µm will change the database size from 25 GByte to net 400 GByte. Storage and communication bandwidth will be the limiting factors. Finally, designs will be assembled in a single location, e.g. the mask centre, where all final design checks are performed.
Process and library development is even today done in parallel with new chip designs. Distributed design environments will rely on distributed concurrent engineering through distributed design project and data management. SoC designs are most often joint design projects between semiconductor and system house design teams, between ASIC customers and ASIC supplier design teams or between cross divisional specialized design teams within the same company, requiring distributed design capabilities. Unfortunately, common design environments today do not provide effective capabilities for such distributed environments.
Short term goals are to establish distributed data management infrastructures. IP catalogs will become widely used. Data security models are urgently required at the project level to cater for multi-site environments.
Future trends are network concurrent design engineering, massive parallel development involving hundreds of persons using several databases and servers at various locations.
Generic applications, like multimedia applications or mixed analogue/digital designs, require concurrent engineering and IP reuse. Data management and distributed IP/design environment will become a competitive advantage.

9. Low Power Design Solutions

The covered topics include synthesis for low power, simulation for low power and system level optimisation for low power.
A major goal is a power driven design methodology, considering especially low power aspects like power and runtime management, multi VDD handling, reliability issues, leakage and timing closure. As a main aspect, this includes the necessity of changes in optimisation criteria, which have to go from speed and size to the consumption and efficiency of power. As long term goals, this will lead to
- power driven synthesis linked to power driven physical design with timing constraints,
- multi-level simulation and stream compaction, and
- complete solutions from system level down to physical implementation.

Especially the last long term goal includes system level runtime management, process optimisation, statistical simulation and optimisation for mixed signal handling, including RF and software aspects.

10. Library production solutions

Future library solutions must address standard, low-power and high-speed designs and will become more and more important. Process development is going at a faster pace while consistency of functional and timing descriptions has to be ensured and the qualification effort has to be reduced at the same time. Many techniques used for library production including characterization and validation will need to be applied to IP as well.
Most beneficial to the enormous task of library production would be a further standardization of views and models. The only way to make that possible is to automate the production flow and using concurrent engineering for technology and library development. Library production automation must be able to quickly generate iterations of standard cells and to allow for outsourcing, design reuse, standardization and standardized EDA environments. The validation of library contents is becoming increasingly complex and time consuming.
The new CMOS technologies require that physical effects are taken into account, also known as deep submicron effects. It will be mandatory to make safe designs with good manufacturing yield. IP packaging can be extremely complex.
Currently, the automation level for memory compilers is still running far behind. Concerning the validation tools for different data and views, we are at the early beginning. The difference between simulated and actual silicon behaviour is increasing. As of today, it is clearly impossible to extract resistors and capacitors of a 4 Mbit memory and to simulate it with any electrical simulation tool.
Short-term goals are to address the validation of all the views contained in a library. Several steps in the validation process can be identified, from unit test to library certification. We have to use powerful database management tools, supporting versioning, module configuration and distributed development environment. Memory compilers are a class in themselves and cannot be treated as standard cells. Interpolation of data from a database of instances is used in estimators in order to get a quick overview of the performance of different configurations. The capacity of extraction and simulation tools must be increased while new tools will be required to validate design and layout choices in a more predictable manner.
Future trends are to separate memory design and memory characterization. Integration of existing macro blocks (IP) to be used as regular library elements in the design flow is necessary. Automation tools have to address the design of library elements.

11. Rapid System Prototyping

Prototyping provides significant technical benefits and economical advantages. The life cycle of new consumer products will be narrower than the development time itself. The overall goal of prototyping is to achieve a system functionality as close to the desired system as necessary for the purposes of validating algorithms/architectures and determining system performance and cost prior to committing to a final solution. Much of the importance of prototyping systems is related to their early availability in the design process. System prototyping has to take into account that some parameters can be different in the final solution, e.g. functionality, system environment and performance.
Prototyping technologies can be classified in virtual prototyping, emulation systems, semi-custom prototyping, custom prototyping, platform-based prototyping, quick turnaround foundries and analog prototyping. The cost of prototyping platforms and the amount of effort necessary to design and bring-up a proto-

type still prevent many companies from using those technologies. Platform-based prototyping seems to be a trend to focus on specific architectures.
Several solutions from major EDA vendors are available today. Except for virtual prototyping solutions, most of the products are oriented towards hardware prototyping. Verification prototyping is currently the most effective solution, and also the less efficient. Many FPAAs (Field-programmable analogue arrays), in system programmable filters and analog building blocks are now available. Fast product prototyping is done by using reprogrammable or configurable hardware such as FPGAs.
Short-term goals should be the improvement of the usability and flexibility of existing platforms together with a reduction in cost. There exists a driving force pushing for faster speed and the ability to integrate (enciphered) IP. A focus should be set on smoothing the path from models to prototypes to reduce the efforts needed to design prototypes. The number of FPGAs in a prototyping system is decreasing: from tens in early '90 to current five/six. Inter-FPGA communication shall be optimised.
Future trends are towards the usage of prototypes to resolve the verification bottleneck and to obtain early product shipment. Virtual prototyping to provide earlier estimation will be reinforced, prototyping platforms will be integrated with simulation environment. Work has to be done on reduction of prototyping platform packaging, improved speed and integration (or interoperability) of prototyping tools, system level design tools and verification tools. The predicted speed for a 2004 verification prototype based on FPGA is 280 MHz. Virtual prototyping is becoming a necessary and high-added-value task in the earlier stage of a design. Reconfigurable analog devices will boost the analogue design process.
Virtual prototyping is suitable for general-purpose computers and embedded system applications. Emulation systems are suitable for CPU and large processor designs for which the validation does not necessitate very high-performance. Semi-custom prototyping provides good performance (up to 30 MHz) and hence can be used to support DSP, telecom and controller design. Custom prototyping and fast turnaround foundries and technologies are dedicated to reactive systems. Place and route tools are necessary to accommodate embedded FPGAs.

12. Test Development for SoC

Testing has become one of the major issues in design and manufacturing. Testing cost may represent up to 50% of the device manufacturing cost. Test-related development should concentrate on tools and methodologies enabling low-cost testing for SoC designs, Hardware/Software co-design, IP- and core-based design, analogue and mixed-signals design and RF on-chip. Another issue is to handle test synthesis at higher design levels to decrease test generation time, area, delay and power consumption overheads and to keep high fault coverage of the overall design. Test specification tools are needed to enforce fast test program development from specification to test programs. Advanced nanometer CMOS technologies demand a move to dynamic test methods and new fault models. Because of the greater variability in the dominating defect mechanisms during process and product ramp-up, test sequences will need to cover a wider set of fault models. Very deep miniaturization tends to make circuits increasingly sensitive to noise, and other spurious defects like soft-errors and timing-faults.
Today, the cost of high-performance ATE per pin is between 5 k and 8 k$. Such testers are needed for at-speed testing. A tester featuring 500 pins may carry a tag of > $ 2 million. Growing pin counts, higher data rates as well as a rising demand for even better accuracy can make testers even much more expensive, maybe up to $ 5 million. Today's tools support test synthesis at gate level, scan, memory BIST and Boundary Scan techniques as well as the stuck-at fault model and IDDQ testing.
Short-term goals are to provide DFT/BIST methods and tools making currently available testers sufficient and economical for SoC testing, to provide DFT and pattern generation tools and to provide methodologies supporting a hierarchical design methodology. There is also a need to introduce test program automation to have production test programs ready within a few days as well as virtual test methods covering even test interface boards to have engineering samples tested 3 days after first silicon release. Further, we need to provide replacements for classical FA tests and screens such as liquid crystal, IDDQ and VSTRESS that will include BIST and BIST with reconfiguration, dynamic test methods, and various delta test methods.
Future trends are towards an executable test specification for test program synthesis methods and new DFT synthesis, which can reduce the cost of ownership of ATE by 10x. Further, test program synthesis and virtual test methods must be established to have engineering samples tested 1 day after first silicon. High-performance, accuracy-balanced behavioural models for DUT, test interface boards and tester instruments are necessary for that purpose. Deep submicron scaling inevitably leads to increased noise sensitivity. Powerful failure analysis mechanisms have to be developed with a resolution down to gate or node level including fully automated failure analysis. BIST techniques for non-volatile memories and new fault models for memory cells should be studied. This will lead to deployment and coupling of advanced dynamic test, diagnosis and debug methods to low-cost test and diagnosis solution for SoC.
Requirements for SoC testing must not ever-increase ATE features and associated price tags. Standardized DFT, BIST, test specification, test program generation and diagnostic approaches are needed to fit all modules well together. The cost for SoC testing must be kept well below the silicon and packaging costs.

13. Packaging

Main evolutions in packaging are observed in the field of interconnect technologies, emerging package families and new materials for environmental purposes.
Interconnect technologies will have to be adapted to new die pad configurations and metallurgies. Die pad pitch reduction requires ever-finer wire bonding techniques. Wire material itself needs in particular cases to have new metallurgy, like copper to ensure a better compatibility with coming copper pads and

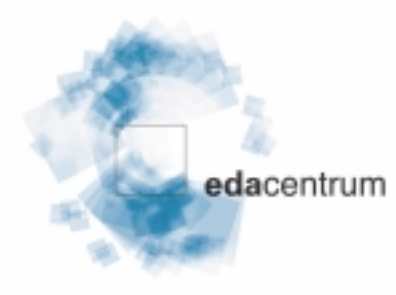
reduce material costs. Flip chip interconnection technology allows a higher density packaging concept, mainly associated with ball grid array (BGA) packages. This often requires higher routing levels on BGA substrates. In order to follow the trend to higher density, improvements in package routing density are required in terms of interposer design tools and manufacturing technologies.

Emerging package families are requested for growing applications: Portable electronic will require new plastic packages (VFQFPN) which are smaller and thinner and which will partially replace well-known plastic packages for size and cost reduction factors. Systems in a package will certainly expand with the need of integrating many functions inside a ball grip array package. This will require 3D structures, possibly mixing interconnect technologies (wire bonding and flip chip).

Environmental purposes will bring packages to lead free solutions, using new matérials such as recyclable or hazard-free types. Modelling and simulation tools will need to integrate into chip design software to provide new key parameters (3D EM-fields, coupling, ground bounce) and cannot longer be analysed separately. Thus, it is a key requirement to interoperate the IC and the package design flow to specify new classes of EDA tools.

Glossary

ASIC	Application Specific Integrated Circuit
ATE	Automatic Test Equipment
BIST	Built In Self Test
BGA	Ball Grid Array
CPU	Central Processor Unit
DFT	Design For Testability
DSM	Deep Sub Micron
DSP	Digital Signal Processing
DUT	Device Under Test
EDA	Electronic Design Automation
EM	Electro Magnetic
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Immunity
FA	Failure Analysis
FPGA	Field Programmable Gate Array
FPAA	Field Programmable Analog Array
HDL	High Level Design Language
IDDQ	Quiescent current – the 'switch-on' current of the device
IEEE	Institute of Electrical and Electronic Engineers
IP	Intellectual Property
MEMS	Micro Electro Mechanical Systems
RF	Radio Frequency
RT	Register Transfer
RTL	Register Transfer Level
SI/EMC/RF	Signal Integrity/Electromagnetic Compatibility/Radio-Frequency
SME	Small and Medium Enterprise
SoC	System-on-Chip
VC	Virtual Component
VDSL	Very high speed Digital Subscriber Line
VDSM	Very Deep Sub Micron
VHDL	Very High Level Design Language
VSIA	Virtual Socket Interface Alliance



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