SOLUTION EXAM DEC 17th, 2013

Surname (readable).....	Name (readable).....
Matr.....	Signature.....

Question Q3

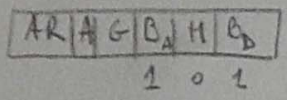
The figure below reports a set of different read/write requests and the arrival time (in cycles) on a shared bus to be served. First you must provide the pipeline Gantt diagram for both a single write and a single read transaction. Second, fill in the available timing Gantt diagram showing the evaluation of the transactions in the system. The following additional conditions are imposed to the system: ***(5 Points)***

- data/address bus are **split**: data bus width is 64 **bits**, address bus width is 64 **bits**
- we do not consider the control bus explicitly
- the payload for each transaction is 64 **bits**
- Transactions have a **FIXED** memory processing time of **1 cycle**
- The architecture implements **PIPELINED** bus
- Each pipeline stage requires 1 clock cycle, but the memory processing defined above
- The arbiter grants **WRITE** first in **FIFO** order
- For each read/write request the arrival time and the request type, i.e. R or W, are provided

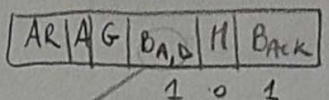
Transactions are granted in a PIPELINE fashion

The grant for the next transaction can be given at the first stage of the previous granted are since the PIPELINE is known by the bus arbiter

READ PIPELINE:

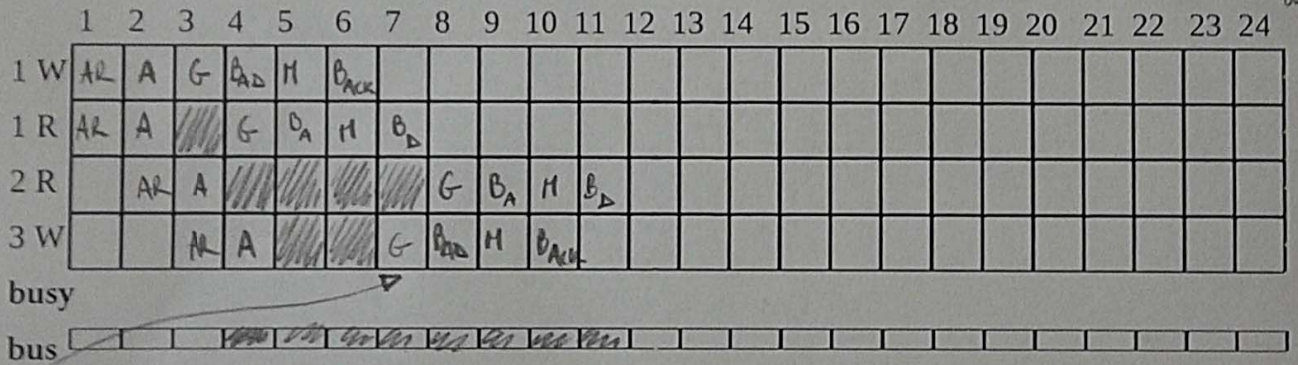


WRITE PIPELINE:



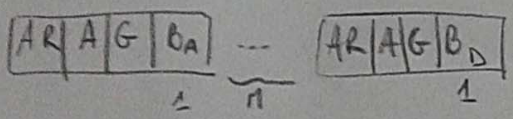
buses are physically split between address and data

Sequence of transactions

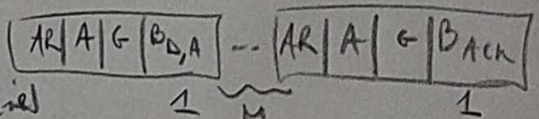


Complete again the exercise considering a **SPLIT** bus, while all the other conditions are the same. ***(5 Points)***

READ PIPELINE:

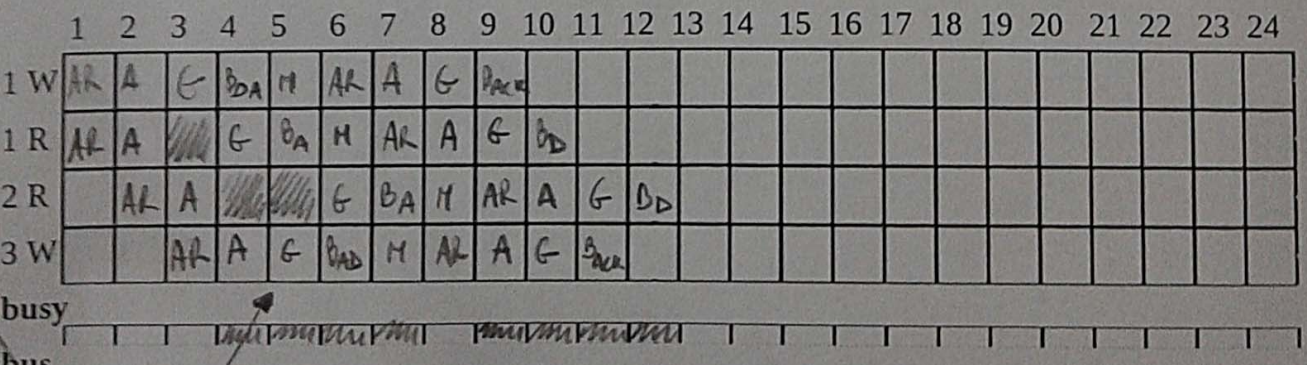


WRITE PIPELINE:



The split pipelined bus can shadow mem accesses even with variable processing time

Sequence of transactions



writes granted FIRST in FIFO order