Politecnico di Milano
FACOLTÀ DI INGEGNERIA DELL'INFORMAZIONE

Sistemi Embedded 1
A.A. 2014-2015 – Exam date: 25 Feb 2015

Prof. William FORNACIARI

Surname (readable).....	Name (readable).....
Matr.....	Signature.....

Q1	Q2	Q3	Q4	TOT

NOTES

It is forbidden to refer to texts or notes of any kind as well as interact with their neighbors. Anyone found in possession of documents relating to the course, although not directly relevant to the subject of the examination will cancel the test. It is not allowed to leave during the first half hour, the task must still be returned, even if it is withdrawn. The presence of the writing (not delivered) implies the renunciation of any previous ratings.

Question Q1

(10 points) *Referring to the Design Space Exploration (DSE), the students is required to discuss:*

- *the main goals and problems addressed by the DSE and the benefits of an automated DSE*
- *what is the concept of robust optimization, possibly with an example*
- *the importance of the analysis metrics and, in particular, the concept of "fidelity"*

Question Q2

a) (3 points) *Describe the concept of event-based simulation. Focusing on GEM5 describe the main event-based infrastructure of the simulator. Why GEM5 implements two different "times"? How does it use them?*

In the event-based simulation everything is governed by software events that mimic real hardware events. An event could be an interrupt, the rising front of the clock etc, that triggers further actions. For example at each rising front of the clock a D flip-flop registers the D value and propagates it to its output Q. In the software an event is an object with an associated time and bound to a function. The function is executed when the event time matches the simulator time. Each clocked hardware module is modeled as as a class in GEM5. Such modules can answer to events and generate events on other objects. They answer to events at each clock cycle, since the clock represents an event itself on all the clocked hardware modules.

GEM5 implements two different concept of time. The clock represents the hardware clock signal that runs up to few GHz and triggers event for all the modules clocked with it.However, multiple clock domain can be present in the same simulated architecture, thus GEM5 implements the second notion of time that is the tick. The tick represents the resolution of the simulator and the common denominator for all the clock signals. The default tick period is 1e-12s.

b) (4 points) *Consider a Network-on-Chip router. Detail the schematic of the crossbar module considering 4 input and 4 output ports using a multiplexer implementation. How, if any, does the increase/decrease in the number of the ports of the crossbar affect its performance ?*

Chapter 4 “Designing network on chip architectures in the nanoscale era”

The increase in the port numbers increase the depth of the multiplexer tree in the crossbar for each outport, thus increases the delay and reduces the maximum achievable frequency

c) (3 points) *Concerning the speculative pipeline implementation of the NoC router details how it works starting from the baseline router pipeline with virtual channels. Moreover, describe the flit types that are affected.*

Baseline router pipeline BW+RC | VA | SA | ST | LT

The speculative SA optimization allows to compute for the same flit the SA and the VA stages at the same time. If both are successful a cycle is saved. However, the VA happens on the head or head/tail flit only, thus providing a benefit for this flit types only.
The maximum benefits of such optimization are obtained with single flit packets, since a cycle out of 5 is saved, at most, whereas the overall benefit decreases with longer packets where only the first flit can save one cycle.

Question Q3

a) (5 points) Given the bus architectural specifications provided in the bullet list below and a set of read write requests, complete the timing diagram and details the pipeline stages for read and write transactions:

- data/address bus are **split**: data bus width is **128 bits**, address bus width is **128 bits.**
- we do not consider the control bus explicitly.
- **PIPELINED transaction model** with the following optimizations:
  [X] SPLIT TRANSACTION [X] BURST TRANSACTION
- Transactions have a **VARIABLE** memory processing time of **[_1_-_3_cycles].**
- Each pipeline stage requires _1_ clock cycle, but the memory processing defined above.
- Arbiter grants in **FIFO** order the transaction that enters A stage first. Split transaction responses have precedence over split requests.
- Timing diagram reports on the Y axis the transactions. For each the arrival time, the transaction type (read or wirte) its payload length and the required memory access time are reported.

READ TRANSACTION STAGES: **WRITE TRANSACTION STAGES:**

Sequence of transactions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
1 W(256,2)	AR	A	G	Bad	Bd	M	M	AR	A	G	Back				
1 R(64,1)	AR	A			G	Ba	M	AR	A		G	Bd			
2 W(128,3)		AR	A			G	Bad	M	M	M	AR	A	G	Back	
2 R(128,1)		AR	A				G	Ba	M	AR	A	G	Bd		

busy bus

Question Q4

(5 points) *Describe and compare polling and interrupt -based I/O in terms of cost, overhead and responsiveness*