Politecnico di Milano
FACOLTÀ DI INGEGNERIA DELL'INFORMAZIONE

Sistemi Embedded 1
A.A. 2014-2015 - Exam date: 16 Dec 2014

Prof. William FORNACIARI

Surname (readable)..... Name (readable).....

Matr..... Signature.....

Q1	Q2	Q3		TOT

1.45

NOTES

It is forbidden to refer to texts or notes of any kind as well as interact with their neighbors. Anyone found in possession of documents relating to the course, although not directly relevant to the subject of the examination will cancel the test. It is not allowed to leave during the first half hour, the task must still be returned, even if it is withdrawn. The presence of the writing (not delivered) implies the renunciation of any previous ratings.

Question Q1

a) Describe the concept of design space exploration (DSE) and robust optimization. In which cases it can be useful? What is the concept of PARETO fronter? Which are the main potential benefits from the industrial standpoint coming from (partially) automated DSE?
b) Metrics are useful to drive DSE; the student is required to explain the concept of fidelity and accuracy of the metrics and their impact on the effectiveness of the design optimization process.

When possible, it is appreciated the reference to practical examples during the explanation.

See slides

ACCURACY

$$A = 1 - \frac{|E(D) - M(D)|}{M(D)}$$

D Design implementation
E(D) Estim. value × metric of D
M(D) Measured × metric of D

FIDELITY

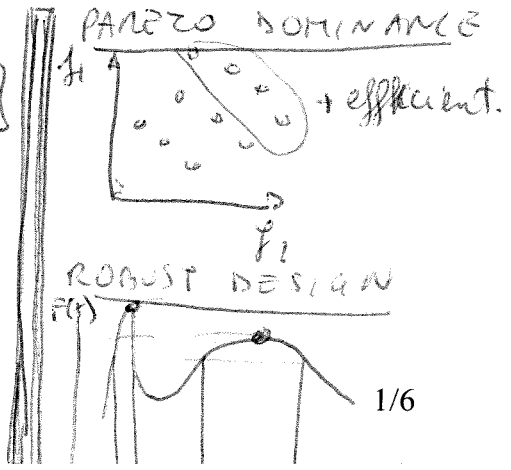
$$F = 100 \cdot \frac{2}{(n-1)n} \sum_{i=1}^{n} \sum_{j=i+1}^{n} M_{ij}$$

M_{ij}: 1 if $E(D_i) > E(D_j)$ and $M(D_i) > M(D_j)$ or $E_i < E_j$ and $M_i < M_j$ or $E_i = E_j$ and $M_i = M_j$; 0 otherwise

Multi obj optimization

$$\max [f_1(x_1 \dots x_2), f_2(\ ), f_3(\ )]$$

subject to $\begin{cases} g_i(x) \le 0 \\ g_j(x) \ge 0 \\ x \in S \end{cases}$



Question Q2

a) (5 points) *GIT defines three different concepts: Working Directory, Staging Area and Committed Project History.*
Describe all of them by focusing on their main differences. Moreover specify the GIT commands to inspect all of them.

b) (3 points) *Given the commit history reported below Fig Q2.b.1 and the list of tracked and untracked files modified/created since the last commit (see List Q2.b.1), specify the correct sequence of GIT commands to generate a new commit including all the files but* ***file2.txt*** *with* ***COMMIT FROM STUDENT*** *as a commit message (see Fig Q2.b.2).*

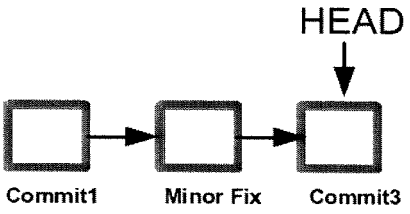


Fig Q2.b.1

Tracked
File1.txt
File2.txt
File3.txt
Untracked
File4.txt
File5.txt

List Q2.b.1

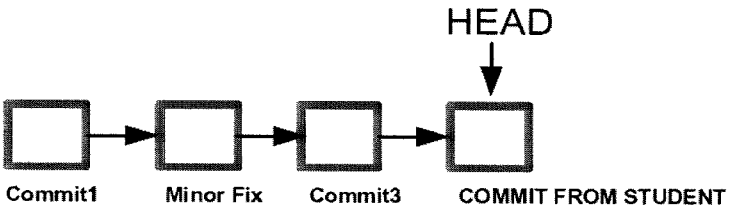


Fig Q2.b.2

c) (2 points) *Starting from the solution at point b you are required to include file2.txt to the last commit without generating a brand new commit, i.e. patching the previous commit. Specify the GIT commands to obtain such an effect.*

SHORT SOLUTION

@ Working directory — starting from a commit (the last if not detached) reports tracked and untracked files that have been modified or created

Staging Area — reports the files that will be added in the next commit

Committed project History — contains the commits with their information i.e. changed files, date, author etc

git status → reports the current Working Directory as well as Staging Area

git log → reports "committed project History" information

git add / reset — to add/remove files to/from the staging area.

(b) git add File1.txt File3.txt File4.TXT File5.TXT
git commit -m "COMMIT FROM STUDENT"

NOTE both modified and untracked files are added in the same way

(c) Stating from the solution in (b)

git add File2.txt
git commit --amend

Note possibility to change again the commit msg.

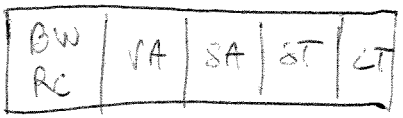
Alternative solution

```
git reset commit3
git add *
git commit -m "COMMIT FROM STUDENT"
```

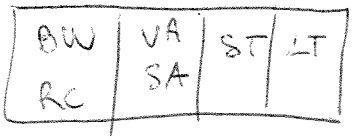
Question Q3

a) (5 points) *Briefly describe the main components (i.e. logic blocks, pipeline stages) of the wormhole Network-on-Chip architecture with Virtual Channels support. How the speculation architectural optimization modifies the pipeline stages and impacts on the round-trip-time if a credit-based flow control scheme is assumed?*

SHORT ANSWER

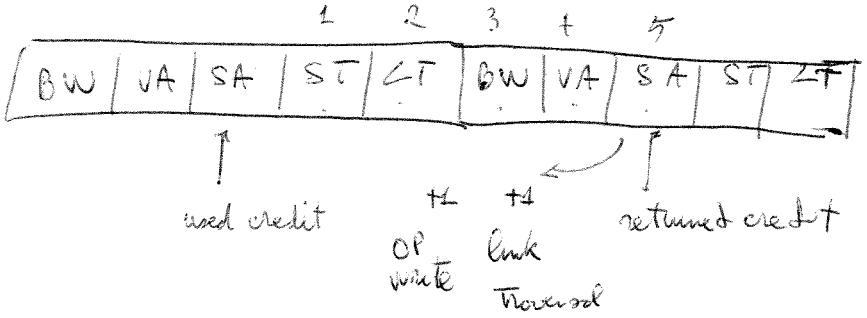


Baseline pipeline



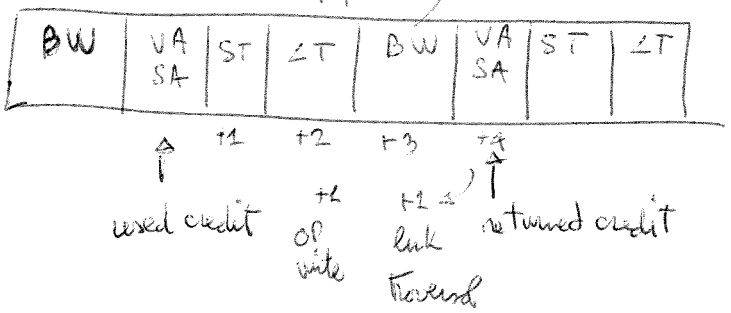
Speculative pipeline

credit round trip time (Baseline pipeline)



reusable ~~after~~ 8 cycles

Credit round trip time (Speculative pipeline)



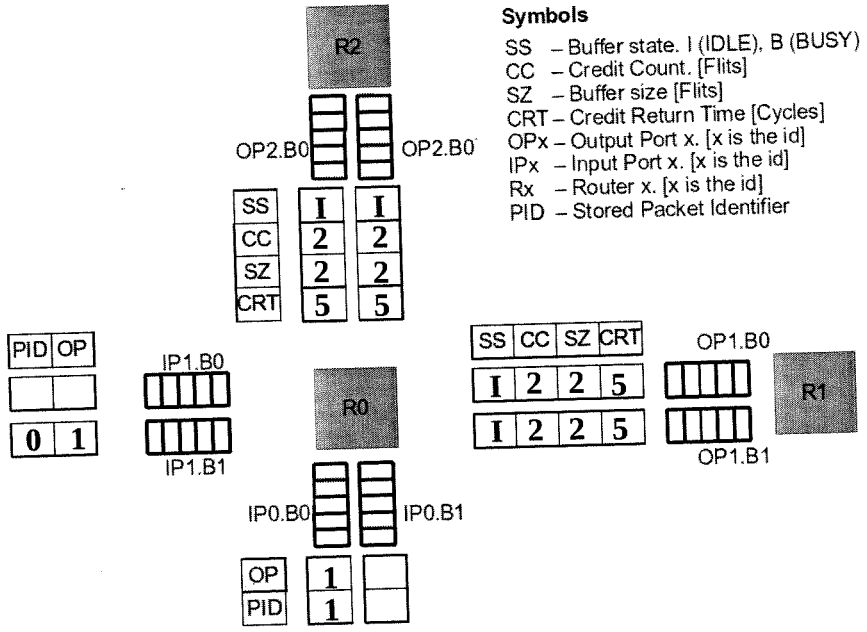
reusable after 7 cycles

Speculation improves CRTT thus allows to reduce buffer size still ensuring full speed/throughput

NOTE missing a block diagram for the baseline considered router architecture. See Textbook suggested on the course website.

b) (5 points) The figure below reports the NoC status at cycle 0, considering three routers. Given the NoC architectural specifications provided in the bullet list below complete the timing diagram below the figure that reports the packet details.

- Router Pipeline: BW+RC | VA | SA | ST | LT
- Input buffers are infinite in size for IP0 and IP1. OP1 and OP2 buffer sizes are reported in the fig (SZ)
- Each packet is supposed to arrive flit by flit one per cycle to the Input Port (IP) starting from the time the HEAD flit is received. For each packet the timing diagram only reports the BW cycle for the HEAD flit.
- **Input buffer info**: stored packet id (ID), requested OP by the stored packet.
- **Output Buffer State**: state (SS), credit count (CC) buffer size (SZ) and the number of cycles a credit takes to return (CRT).
- The VA can grant up to a single IBUF per IP and per OP per cycle, using a round robin allocation strategy. Lowest ID is granted first at the very first RR decision.
- The SA uses a round robin allocation strategy (IP0 first) and a FLIT switching strategy. Lowest ID is granted first at the very first RR decision
- **Assume Atomic Virtual Channel Allocation. Both SA and VA use two-stage arbitration input-first.**



		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
[IP1.IB1]	**H0**	BW	–	VA (1)	SA (1)	ST	LT			●															
(reqOP=1)	**B0**		BW			–	SA (0)	ST	LT			●													
	T0			BW				–	–	SA (0)	ST	LT			●										
[IP0.IB0]	H1	BW	VA (0)	SA (1)	ST	LT			●																
(reqOP=1)	B1		BW		–	SA (0)	ST	LT			●														
	T1			BW			–	–	SA (0)	ST	LT			●											

Comments and notes for the lecturer (OPTIONAL)

PKT 0
cycle 2 | H0 VA conflict VA.OP
5 | D0 SA conflict SA.OP
7,8 | T0 SA credit count is 0

PKT 1
cycle 4 | B1 SA conflict SA.OP
6,7 | T1 SA conflict and credit count is 0