Experimental Behavior of a Two-Chip Charge Amplifier for High-Stability Spectroscopy Systems

Marco Sampietro, Member, IEEE, Chiara Guazzoni, Member, IEEE, Hermes Cruciatia, and Peter Lechner

Abstract—We present the first experimental characterization of an innovative two-chip detector system for X-ray spectroscopy experiments in which stability of operation is mandatory to avoid on-line calibration procedures. The system is based on a silicon drift detector and on a charge amplifier partly integrated in the detector chip. The design guidelines of both the “detector chip” produced on a high resistivity substrate and the “amplifier chip” designed in 0.8-μm BiCMOS technology are reviewed. The proper functionality of each of the two chips and the performance of the whole system have been experimentally verified.

Index Terms—Charge amplifier, high stability, X-ray spectroscopy.

I. INTRODUCTION

In the last decade, big efforts have been devoted to enhance the energy resolution of silicon detectors while extending their active area. This trend has led to the development of silicon drift detectors and their parental devices [1]–[3] and to the integration of the first stage of the front-end electronics on the detector chip [4].

Our work follows this trend and aims to improve with respect to the available solutions the stability of the charge-to-voltage conversion when temperature, bias, or rate varies during experiments and recalibration procedures are difficult to perform. To accomplish this task, we have designed a charge amplifier configuration [5] in which:

1) the amplifier components that are directly connected to the detector anode have been integrated on the detector chip, in order to minimize parasitic capacitances and to obtain the capacitive matching between the detector and the input transistor;

2) all other components of the transimpedance amplifier that close the feedback loop have been integrated in a 0.8-μm BiCMOS chip.

The first experimental results obtained with this two-chip system are the subject of this paper. Section II will briefly review the design and the layout of the two chips and will present the dc characteristics of the devices integrated on the detector chip, to demonstrate that the embedded front-end devices behave properly. Section III is devoted to the experimental characterization of the whole system with particular attention to the behavior of the MOS reset device and to the first experimental evidence of the improved stability in the charge-to-voltage conversion of this first prototype with respect to a source follower configuration. In Section IV, we draw our conclusions and illustrate our future plans.

This work is complementary to the efforts toward the same goal of achieving maximum energy resolution devoted by other groups [6], [7] to design a single CMOS chip that implements the whole preamplifier to be connected to a detector chip without integrated electronics. Both solutions have advantages and drawbacks and are giving interesting results. Our solution, which is technologically more challenging, can be more advantageous in the case of a multi-anode system thanks to the lower sensitivity to the parasitic capacitance added by the off-chip connection.

II. DESIGN AND FUNCTIONALITY OF THE TWO CHIPS

The two-chip system is shown in Fig. 1, where the electrical schematic of the transimpedance amplifier is also visible. The front-end nJFET, the feedback capacitance, and the MOS reset transistor are integrated in the detector chip. The other components of the charge amplifier are integrated in a second chip designed in BiCMOS technology and bonded to the detector chip.

The design of the detector embedded system has to face the technological constraints associated with the limited production steps used for the detector. The starting material is a high-resistivity (2 kΩ-cm) n-type detector-grade silicon wafer. In Fig. 2, a closeup of the layout of the central region of the designed detector is shown. The circular symmetry front-end nJFET is located inside the anode ring and is separated from the anode ring by a p+ guard ring reverse biased with respect to the n-type bulk. The reset transistor is embedded within the input JFET with no changes in the anode ring dimensions by reducing the effective JFET perimeter. The real input JFET is within the bold line in Fig. 2.

The innovative part of the design stands in the use of a p-MOSFET as reset device in parallel to the feedback capacitance and operated in subthreshold conditions. The p-MOSFET drain coincides with the gate of the nJFET while the source is obtained with a p+ implant that faces the drain. The gate
Fig. 1. Schematic of the two-chip charge amplifier. All elements directly connected to the detector anode are integrated on the detector chip to obtain maximum performance (the detector chip is shown with a gray background). The amplifier chip integrated in a conventional BiCMOS technology contains a transimpedance amplifier properly designed to cope with the characteristics of the on-chip JFET of lower transconductance than commercially available JFETs.

Fig. 2. Layout of the detector embedded front-end with a p-MOS transistor for the continuous reset of the feedback capacitor. The outer ring is the detector anode. The pMOSFET aspect ratio is about one.

of the p-MOSFET is a metal strip over the oxide. In the leakage current range below 1 nA, typical for high-resolution silicon detectors, like silicon drift detectors, the p-MOSFET in subthreshold conditions is expected to add the minimum noise, very close to the shot noise of the detector leakage current, and to give an output shape close to an ideal exponential discharge. These advantages of the use of the p-MOSFET in subthreshold regime as a reset element in charge amplifiers are dealt with in [8]. The feedback capacitance (50 fF) is obtained with a metal contact over the nitride layer placed on top of the anode ring implant. The contribution of stray capacitances has been reduced to less than 1% the value of the feedback capacitance in order to achieve the maximum stability in the charge-to-voltage conversion.

The dc characteristics of both the input nJFET and the reset pMOS transistor have been measured with both the devices properly biased in order to test the joint operation of the detector embedded front-end. The characteristic curves of the integrated JFET are shown in Fig. 3. The saturation current is 792 μA, the transconductance at 4 V drain-to-source voltage and 0 V gate-to-source voltage is about 310 μA/V, and the dynamic output resistance is 18 kΩ, properly suited to our application.

The transimpedance amplifier has been designed to provide an adequate loop-gain and bandwidth when coupled with the low transconductance of the front-end nJFET and with the parasitic capacitance that the off-detector-chip connection imposes. Let us shortly review the design of the amplifier by referring to Fig. 1. The input of the transimpedance amplifier is a transistor in common gate configuration. This cascode configuration is biased by a symmetrical divider that provides a fixed voltage of 6 V to the gate of the cascode independently of temperature variations. The MOSFETs in the divider lower the divider output
impedance to less than 1 kΩ, thus minimizing the injected noise.
The current variation in the divider due to temperature variations is collected by the transistor M7 in the tail of the symmetrical divider and mirrored to the two following stages of M11 and Q1. By choosing a mirroring ratio equal to the ratio $R_2/R_5$, the voltage drop across $R_5$ tracks the temperature and reduces to a minimum the dc drift of the gain node.

The open-loop response of the transimpedance amplifier has been measured in the temperature range of $-40$ to $+20$ °C to be of about 750 kΩ with a gain bandwidth product of 105 MHz.

The measured rise time (when coupled with the on-chip input JFET) is 18 ns at room temperature (20 °C) and lowers to 15 ns at $-40$ °C, mainly due to the increase of the transconductance of the nJFET.

### III. EXPERIMENTAL CHARACTERIZATION

#### A. Reset MOSFET Working Performance

The compensation of the electrons collected at the anode is made by means of a MOSFET device in the feedback loop (see Fig. 1). It is dc coupled and is biased in subthreshold regime to perform a continuous reset. The MOSFET ($W/L \approx 1$) is embedded in the JFET transistor structure, having an independent source connected to the output of the preamplifier chip. The gate of the MOSFET is held at a fixed potential. Any increase of leakage electrons at the anode produces an increase in the amplifier voltage that forces the MOSFET source to inject more holes in the MOSFET channel. These holes are collected by its drain, which is the same implant of the JFET gate. A cross section of the reset structure is shown in Fig. 4.

Fig. 5 shows the time behavior of the output voltage of the preamplifier when the leakage current from the detector is varied by means of a variation of the visible light impinging on its sensitive area. The ability of the reset MOSFET to modify its working point to accommodate new experimental conditions is clearly visible. The equivalent resistance useful for the feedback capacitor discharge is given by the inverse of the MOSFET transconductance. The compensation of a very low leakage current (dark condition in the figure), corresponding to an equal low current in the reset MOSFET, produces a very high equivalent resistance across the reset MOSFET. As a consequence, the feedback capacitance discharges with a long time constant. When light is increased, higher leakage currents are generated. The reset MOSFET senses the current variation and updates its bias point in order to be able to compensate that current. The corresponding higher transconductance is mirrored in a faster decay time of the output pulse.

#### B. Reset Dynamic Range

The MOSFET active reset system has a very large dynamic range for leakage current compensation. Many orders of magnitude of leakage current variations produce a variation of the output voltage of only few hundreds of millivolts. In our case, as shown in Fig. 6, a variation of about 400 mV of the amplifier output can accommodate leakage currents varying from 1 pA up to about 4 nA. This feature is made possible by the logarithmic relationship between the current in the reset MOSFET and the gate-source voltage when the MOSFET is operating in subthreshold regime. Such a wide dynamic range in the reset current avoids continuous trimmer of the setup when temperature or detector bias changes from one measurement to the other. The fitting of the experimental points is exponential, indicating that the reset MOSFET is truly working in its subthreshold regime.

A drawback of the variation in the discharge time constants is that the following pole-zero compensator should be dynamic. This is relatively easily accomplished nowadays by digital adaptive filtering [9], [10] or by analog techniques that...
sense-and-replay the reset current into the following pole-zero stage [6], [11]. However, the effect of a nonexact adjustment of the pole-zero compensator has negligible influence on the achievable energy resolution.

C. Linearity of Discharge

The fact that the reset device sets its equivalent resistance on the actual flowing current implies that also the charge carried by each pulse produces a variation of the MOSFET transconductance and, consequently, a variation of the discharge time constant along the pulse itself. This effect is nevertheless very small in our range of operation. Fig. 7(a) shows the output response of the amplifier for input pulses given by a 5-keV photon and by a 25-keV photon when the standing leakage current is very small (dark ambient condition $I_{\text{leak}} < 10$ pA). Fig. 7(b) shows the output response to the same input signals when the standing leakage current is much higher than in normal operating conditions ($I_{\text{leak}} > 1$ nA), obtained by strong illumination of the detector active area. Both figures show how small is the change in shape of the preamplifier discharge despite the full-signal amplitude sweeps up to 25 keV, which is already the upper limit of conversion efficiency of a 300-μm-thick silicon detector.

The small variation that can be noticed in Fig. 7(b) is mainly due to the fact that the reset MOSFET is leaving a strong subthreshold regime and entering an inversion regime [8].

D. Stability of Amplification

First experimental measurements are confirming the expected amplification stability of the proposed configuration under detector bias variations. The experiments are made by taking $^{55}\text{Fe}$ spectra at different bias conditions and by measuring the corresponding peak shifts. In the case, for example, of about 80% variation of the bias voltage of the first ring around the anode from 5 to 9.2 V that produces a variation of the detector capacitance of few percent (see [12, Fig. 5]), the spectrum peak has only shifted by 0.06%.

IV. CONCLUSION AND PERSPECTIVES

The first experiments on the proposed two-chip system performing a charge amplification are confirming the validity of the project and are showing that stabilities below 0.1% in the charge amplification can be reached. Experiments under varying temperature and rate conditions are foreseen in the next months to definitely validate the system.

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