Antonio Rosario Miele

Full name	Antonio Rosario Miele
Date of birth	30/07/1981
Place of birth	Avellino
Citizenship	Italian
Spoken languages	Italian (native), English (fluent)
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Highlights

- Assistant professor (senior) at Dipartimento di Elettronica e Informazione, Politecnico di Milano since June 2018 (according to the Italian Law n. 240/2010 - art. 24, par. 3, letter B); Assistant professor (junior) for 4 years; 4 years post-doc research experience.
- Italian National Scientific Qualification to the function of Associate Professor in Information Processing Systems (09/H1 - Sistemi di Elaborazione delle Informazioni), obtained on April 4, 2017.
- Author of 4 papers in IEEE Transactions on Computers, 2 papers in IEEE Transactions on VLSI Systems, 1 paper in IEEE Design & Test and 1 paper in Elsevier Information Systems journal. In total author of 14 journal papers, 2 editorial contributions, 4 book chapters, 44 conference papers and 4 workshop papers.
- 1 Best Paper Award at the Int. Symp. of Defect and Fault Tolerance in VLSI Systems, in 2010.
  1 Best Demo Award at the Reconfigurable Architecture Workshop, in 2016.
- H-index: 15 ⋄ Total citations: 838 (src: Google Scholar, June 5, 2018).
  H-index: 12 ⋄ Total citations: 572 (src: Scopus, June 5, 2018).
- Program co-Chair of the IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems for 2 editions, in 2016 and 2017. Topic co-Chair of the Track A6 at Int. Conf. on Design Automation & Test in Europe in 2018 and 2019. Participation to the Technical Program Committee of 10 conferences and 2 workshops during the last year.
- Guest co-Editor for a Special Issue/Section of the IEEE Transactions on Emerging Topics in Computing in 2016-2017 and a Special Session of the IET Computers & Digital Techniques in 2018.
- Contribution to 3 European Projects and 1 national one. In particular, Task leader in the SAVE European Project, and primary researcher in specific task activities in the other projects.
- Recent ongoing research collaboration with Prof. A. Rahmani's research group (University of Turku, Finland) on the "reliability-aware runtime resource management for many-cores in the dark silicon era" topic, leading to several publications.
- Starting from 2013-2014, 1 course taught per academic year at Politecnico di Milano: Computer Science Fundamental (Undergraduate course for Electrical Engineering degree: 150+ students till to 2015-2016, Undergraduate course for Civil Engineering degree: 300+ students in 2016-2017). Starting from 2006-2007, 2+ courses as teaching assistant per academic year at Politecnico di Milano. 3 different Ph.D. courses taught at Politecnico di Milano in 2015-2016 (15+ students), in in 2016-2017 (10+ students) and in 2017-2018 (30+ students). 1 Ph.D. course taught in 2016 at the University of Turku, Finland (20+ students).

Profile

Antonio Miele has been initially involved in research activities during his B.Sc. studies, when working on his graduating thesis on the design of a very-small portable light DBMS (dubbed PoliDBMS), as part of the MIUR-FIRB MAIS project; the work was presented in a paper at a national conference on database systems. During the M.Sc. studies, he started contributing regularly to research activities, under the supervision of Prof. Cristiana Bolchini, in the field of dependable systems design, with a specific focus on the definition of software and hardware techniques for the hardening of reliable microprocessors working in harsh conditions. This field of research has become his major interest topic pursued during the Ph.D. studies and post-doc activities. More precisely, Antonio Miele investigated methodologies and developed tools for the design and analysis of dependable computing systems, covering a wide spectrum of scenarios. During the Ph.D. he proposed solutions for the design fault tolerant embedded systems, as well as to evaluate their reliability-related properties by means of fault injection strategies. Such solutions have been devised for reconfigurable architectures, such as those implemented on SRAM-based FPGAs (commonly used in space-mission applications), as well as for heterogeneous distributed multiprocessor systems (such as the ones adopted in the automotive scenario), working at different levels of abstraction. Design space exploration and optimization strategies are at the center of these research activities, aiming at identifying solutions for the given problems; nevertheless, these strategies have been designed in a flexible way to be exploited also in different application scenarios.

During the post-doctoral period and the subsequent position as assistant professor, these same research interests have been broadened to take into account a more dynamic adaptable application environment, more appropriate for today and tomorrow computing scenario. In particular, his effort is devoted to self-adaptive computing systems, for both reliability-related goals (such as fault mitigation and aging management) and performance/energy optimization ones (stemming from the involvement in the SAVE EU project). From the architectural point of view, Antonio Miele's competences span from traditional embedded systems, to reconfigurable FPGA-based systems and heterogeneous multi-core and many-core system architectures.

Today, Antonio Miele has a strong background on design methodologies for embedded systems, and on dependability-related issues of digital systems, with a growing interest in self-adaptive computing systems. Moreover, the methodological approach usually adopted to tackle the specific problems allowed him to grow a body of competences that can be exploited within a broader scenario and led to his active involvement in 4 research projects. He has been one of the main scientific contributors of the local research unit for the MIUR-PRIN project on "High reliability fault tolerant digital systems in nanometric technologies: characterization and design methodologies"; the outcome is a methodology and companion tool for the design of fault tolerant systems onto SRAM-based FPGAs. His expertise on multi-core system simulation has been exploited in SCALOPES, SMECY and SAVE EU projects, where three simulation tools have been developed. In the SCALOPES project, he contributed to the implementation of a simulation environment to support the performance and reliability evaluations of multiprocessor architecture provided with reconfigurable hardware accelerators. In the SMECY project, he developed another system-level simulator for multi-core architectures and employed it to define and validate novel adaptive reliability-aware strategies for mitigating the effects of the faults in software execution. Finally, for the SAVE project, Dr. Miele led the task for the development of a virtual platform for the simulation of heterogeneous system architectures, for exploring runtime resource management, suitable for performance/energy trade-offs. In the same project, he actively contributed to the design and validation of novel runtime resource management policies for heterogeneous multi-core architectures.

Antonio Miele has also actively contributed to the MEDIAN EU Cost Action, establishing new international relationships and joint research activities, in particular with Prof. M. Psarakis (University of Piraeus - Greece) and Prof. A. Rahmani (University of California, Irvine - US; previously, University of Turku - Finland). Scholarships were awarded to support brief stays to strengthen the collaboration.

All these research activities have led to the publication of about 60 papers on peer-reviewed journals and proceedings of international conferences. For his competences he has been invited in technical program committees of conferences in the area of reliable and reconfigurable systems (e.g., DATE, DFT, FPL, IOLTS); moreover, he served as program co-chair for the DFT symposium in 2016 and in 2017, and he is currently serving as topic co-chair for the DATE conference since 2018, and as a guest editor for a special issue in the IEEE Transactions on Emerging Topics in Computing in 2017 and for another special issue in IET Computers & Digital Techniques in 2018.

Finally, the collaboration with prof. Letizia Tanca and her research group started with the B.Sc. thesis has been later continued (as a secondary research during the Ph.D. studies and post-doc period) covering the definition of methodologies for the personalization and the reduction of context-dependent data views.

Position and Education

Record of Employment

June 2018 –present

Assistant professor at Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, (according to the Italian Law n. 240/2010 – art. 24, par. 3, B).

May 2014 –May 2018

Assistant professor at Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, (according to the Italian Law n. 240/2010 – art. 24, par. 3, A).

March 2014 – April 2014

Temporary research assistant at Dipartimento di Elettronica, Informazione e Bioingegneria of Politecnico di Milano working on "Design and implementation of a virtual platform for the simulation of heterogeneous architectures".

March 2012 – February 2014

Temporary research assistant at Dipartimento di Elettronica, Informazione e Bioingegneria of Politecnico di Milano working on "Methods and techniques for the design of reliable many/multi-core architectures".

March 2011 – February 2012

Temporary research assistant at Dipartimento di Elettronica e Informazione of Politecnico di Milano working on the "Definition of an approach for fault mitigation in sRAM-based FPGA devices by means of partial reconfiguration".

March 2010 – February 2011

Temporary research assistant at Dipartimento di Elettronica e Informazione of Politecnico di Milano working on the "Definition of a strategy for fault injection for the reliability analysis of SystemC models using ReSP platform".

January 2007 – December 2009

Ph.D. student at Dipartimento di Elettronica e Informazione of Politecnico di Milano.

September 2006 – December 2006

Temporary research collaborator at Dipartimento di Elettronica e Informazione of Politecnico di Milano working on the "Analysis of power consumption of flash memories in wireless sensor networks".

Qualifications

- Italian National Scientific Qualification to the function of Associate Professor in Information Processing Systems (Italian academic discipline code: 09/H1 - Sistemi di Elaborazione delle Informazioni), from the Italian Ministry of Education, Universities and Research (MIUR). Obtained on April 4, 2017 according to article 16, subsection 1, of the Italian law number 240/10.
- Italian Professional Qualification to the function of Engineer (Esame di Stato per l'abilitazione alla Professione di Ingegnere). 2006.

Education

- Ph.D. in Information Technology at Politecnico di Milano (*European Ph.D. Certification*). March 2010.
  Thesis title: *A methodology for the design and the analysis of reliable embedded systems*, Advisor: *C. Bolchini*, Reviewers: *R. Leveugle (TIMA Laboratory, France) and D. Gizopoulos (University of Piraeus, Greece)*
- M.Sc. in Computer Science at University of Illinois at Chicago. July 2006. GPA: 3.71/4.00.
  Thesis title: *A software approach for hardware/software co-design of reliable embedded systems*, Advisor: *D. Sciuto*
- M.Sc. in Computer Engineering at Politecnico di Milano. July 2006. Grade: 110/110.
  Thesis title: *An analysis of software techniques for the design of reliable embedded systems*, Advisor: *C. Bolchini*
- B.Sc. in Computer Engineering at Politecnico di Milano. September 2003. Grade: 103/110.
  Thesis title: *Portable DBMS: design and implementation of an SQL Parser*, Advisor: *C. Bolchini*
- Scientific high school diploma from Liceo Scientifico "Elio Vittorini" (Milano). 2000. Grade: 94/100.

VISITING EXPERIENCES

- University of Turku, Finland (1 week in Feb. 2016), funded by the University of Turku.
- University of Turku, Finland (1 week in Feb. 2015), grant from the Cost Action no. IC1103, MEDIAN.
- University of Piraeus, Greece (1 week in Feb. 2014) grant from the Cost Action no. IC1103, MEDIAN.
- European Space Agency, ESA/ESTEC in the Netherlands (3 months, Sept. 2008 - Dec. 2008).

SCHOLARSHIPS

- Ph.D. scholarship from Italian Ministry of Education, University and Research (Jan. 2007 - Dec. 2009).

Teaching activities

The following teaching activities have been carried out at Politecnico di Milano except where otherwise stated below. Teaching evaluations for courses of the last academic years as reported, when available.

2017-2018

Advanced Topics on Heterogeneous System Architectures (*Lecturer*, with Dr. M. Santambrogio) - Ph.D. in Information Technology - Ph.D. level.

Informatica (*Lecturer*) - Civil Engineering - Undergraduate level.
(**Global teaching evaluation: 3.48/4 – School average value: 3.08/4**)

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level.
(**Global teaching assistant evaluation: 3.51/4 – School average value: 3.11/4**).

2016-2017

Advanced Topics on Reconfigurable FPGA-based Systems Design (*Lecturer*, with Dr. M. Santambrogio) - Ph.D. in Information Technology - Ph.D. level.

Informatica (*Lecturer*) - Civil Engineering - Undergraduate level.
(**Global teaching evaluation: 3.40/4 – School average value: 3.04/4**)

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level.
(**Global teaching assistant evaluation: 3.38/4 – School average value: 3.13/4**).

2015-2016

Heterogeneous System Architectures (*Lecturer*) - Ph.D./master course taught at **University of Turku, Finland**.

Advanced Topics on Heterogeneous System Architectures: architectures, programming models and resource management (*Lecturer*, with Dr. M. Santambrogio) - Ph.D. in Information Technology - Ph.D. level.

Informatica B (*Lecturer*) - Electrical Engineering - Undergraduate level.
(**Global teaching evaluation: 3.30/4 – School average value: 3.10/4**).

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level
(**Global teaching assistant evaluation: 3.27/4 – School average value: 3.12/4**).

2014-2015

Informatica B (*Lecturer*) - Electrical Engineering - Undergraduate level
(**Global teaching evaluation: 3.25/4 – School average value: 3.08/4**).

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level
(**Global teaching assistant evaluation: 3.65/4 – School average value: 3.11/4**).

2013-2014

Informatica B (*Contract lecturer*) - Electrical Engineering - Undergraduate level
(**Global teaching evaluation: 3.25/4 – School average value: 3.06/4**).

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level
(**Global teaching assistant evaluation: 3.18/4 – School average value: 3.08/4**).

2012-2013

Informatica B (per aerospaziali) (*Teaching assistant*) - Aerospace Engineering - Undergraduate level.

Fondamenti di informatica (*Teaching assistant*) - Computer Engineering - Undergraduate level.

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level.

Fondamenti di informatica (*Lab. supervisor*) - Computer Engineering - Undergraduate level.

2011-2012

Dependable systems (*Teaching assistant*) - Computer Engineering - Graduate level.

Informatica B (per aerospaziali) (*Teaching assistant*) - Aerospace Engineering - Undergraduate level.

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level.

Fondamenti di informatica (*Lab. supervisor*) - Computer Engineering - Undergraduate level.

2010-2011

Informatica B (per aerospaziali) (*Teaching assistant*) - Aerospace Engineering - Undergraduate level.

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level.

Fondamenti di informatica (*Lab. supervisor*) - Computer Engineering - Undergraduate level.

2009-2010

Reti logiche (*Teaching assistant*) - Computer Engineering - Undergraduate level.

Fondamenti di informatica (*Lab. supervisor*) - Computer Engineering - Undergraduate level.

2007-2008

Informatica B (informatica per applicazioni scientifiche ed industriali) (*Teaching assistant*) - Physics Engineering - Graduate level.

Laboratorio software (*Teaching assistant*) - Computer Engineering - Graduate level.

2006-2007

Informatica B (informatica per applicazioni scientifiche ed industriali) (*Teaching assistant*) - Physics Engineering - Graduate level.

Informatica B (*Teaching assistant*) - Mechanical Engineering - Undergraduate level.

2005-2006

Ingegneria del software (*Lab. tutor*) - Computer Engineering - Undergraduate level.

2004-2005

Ingegneria del software (*Lab. tutor*) - Computer Engineering - Undergraduate level.

Informatica 1 (*Lab. tutor*) - Computer Engineering - Undergraduate level.

2003-2004

Informatica 2 (*Lab. tutor*) - Computer Engineering - Undergraduate level.

Informatica 1 (*Lab. tutor*) - Computer Engineering - Undergraduate level.

Graduate Students Advisor

- *Stefano Bielli*, "QRRMS: A Q-learning-based Runtime Resource Management System for Heterogeneous Multicore Architectures", 2015.

Graduate Students Co-Advisor

- *Clara Casas Castedo* (Erasmus student), "Hardened HW/SW systems implemented on Zynq-7000 boards", 2013.
- *Miguel Baquero Gago* (Erasmus student), "Performance-aware HW/SW systems onto Zynq-7000 boards", 2013.
- *Renzo Cancho*, "Evaluating Different Solutions for Hardening Floating Point Units", 2013-ongoing.
- *Naser Derakhshan* (Erasmus student), "Dependable Configuration Controller for Multi-FPGA Platforms", 2012.
- *Luca Cerri*, "Una strategia di mapping dinamico per applicazioni su piattaforme many-core", 2012.
- *Stefano Guidobaldi*, "E-SWEAM: una metodologia per l'analisi di guasto all'interno di applicazioni eseguite su sistemi dedicati", 2011.
- *Emanuele Rabosio*, "Applicazione di tecniche di data mining per l'estrazione di preferenze contestuali", 2009.
- *Fabrizio Castro*, "Progettazione e sviluppo di un sistema per l'iniezione di guasti in dispositivi FPGA per l'analisi di affidabilità", 2009.

Ph.D. Students Supervision

Dr. Miele has contributed to the supervision of the following Ph.D. students during their research activities:

- *Anil Kanduri*, Ph.D. student at the University of Turku, Finland, 2015-ongoing.
- *Mohammad Hashem Haghbayan*, "Energy-Efficient and Reliable Computing in Dark Silicon Era", University of Turku, Finland, 2014-ongoing.
- *Matteo Carminati*, "Towards the definition of a methodology for the design of tunable dependable systems", Politecnico di Milano, 2012-2014.
- *Chara Sandionigi*, "A reliability-aware design methodology for embedded systems on multi-FPGA platforms", Politecnico di Milano, 2009-2011.

Moreover, Antonio Miele has supervised thesis activities of about 10 undergraduate students, and project activities of more than 70 undergraduate, graduate and Ph.D. students for various courses (Dependable Systems, High Performance Processors and Systems, Advanced Computer Architectures, Progetto di Ingegneria Informatica, Advanced Topics on Heterogeneous System Architectures, Advanced Topics on Heterogeneous System Architectures, Advanced Topics on Reconfigurable FPGA-based Systems Design).

Research interests

Dr. Miele's research interests can be organized into two different lines presented in the following sections: the main one deals with methodologies for the design of reliable computing systems, and the other one with methodologies for the personalization of context dependent data views.

METHODOLOGIES FOR THE DESIGN AND THE ANALYSIS OF RELIABLE COMPUTING SYSTEMS

Reliability aspects play a relevant role in computing systems' design, not only in mission-critical application scenarios as traditionally occurred, but also in more common environments, due to their pervasiveness in today's life. Moreover, the susceptibility of digital systems to faults, both transient ones mainly caused by environmental phenomena (such as radiations) and permanent ones due to aging and wear-out effects, has increased due to the aggressive technological scaling. Being the problem not new, although becoming more and more relevant, literature offers a wide set of reliability-oriented design techniques, devoted to the introduction of fault detection or tolerance properties in the system. However, the common practice of considering the system hardening step and the reliability analysis separately from the main design flow (as typically done in the embedded systems' design scenario) does not suffice, because of the many issues the designer has to face with (e.g. increasing system complexity, stringent time-to-market and cost requirements).

The goal of Dr. Miele's research is the study of new methodologies for the *design* and the *analysis* of computing systems (in particular, embedded and mobile ones) with reliability requirements. These methodologies deal with system reliability issues right from the beginning of the design flow, and include them as part of the overall process with a holistic approach; in this way, it is possible to drive the numerous decisions by exploiting the synergy of both classical aspects and reliability-oriented ones. In these years, different architectures and technological platforms have been considered (from traditional embedded systems to reconfigurable FPGA-based systems and heterogeneous multi-core and many-core system architectures), proposing hardening methodologies and tools enabling the system to autonomously detect the occurrence of a fault and possibly mask/mitigate its effects. In the recent years, this interest has evolved towards i) the design of self-adaptive reliable systems, able to dynamically adapt to the occurrence of faults, also considering the varying conditions of the working environment, and ii) the handling of device wear-out issues, that can be effectively mitigated by means of suitable workload distribution strategies in order to balance the aging trend of the various processing resources. The key issues tackled by this broad-spectrum research are discussed in the following.

Reliability-driven system-level design. The standard system-level design flow for embedded systems has been enhanced to support the management of reliability issues and, in particular, the automated introduction of reliability mechanisms. The defined methodology enables an automated two-step design space exploration for the selection of the hardening techniques and, then for the system-level synthesis of the obtained reliable system specification. The goal of the methodology is the identification of a reliable system implementation able to fulfill the reliability requirements specified by the designer and at the same time with a reduced overhead due to the hardening techniques on the implementation costs and performance. Recently, aging and wear-out issues have being taken into account in the optimization process in order to prolong system lifetime reliability. The research products are a set of software frameworks automating the design

space exploration [SW.4] and the evaluation of the lifetime reliability of a system [SW.3], and the following publications: [IC.1], [IC.2], [IC.6], [IC.14], [IC.18], [JR.9], [IC.29], [IC.30], [JR.14], [IC.41] and [IC.42].

Self-adaptive heterogeneous multi-/many-core systems. This study aims at defining new strategies and mechanisms for enabling self-adaptiveness in heterogeneous multi-/many-core architectures, particularly focusing on reliability issues. The research investigates the design of systems with a "tunable" level of reliability, balanced with respect to performance and costs. More precisely, the level of reliability can be adapted at run-time based on the explicit user's request or, implicitly, according to the execution context by varying a set of knobs offered by the reliability-oriented mechanisms (e.g., the number of execution replicas or the numbers of checkpoints). The research focuses also on runtime resource management approaches for mitigating the aging effects in multi-/many-core architectures with the aim of prolonging the system's lifetime while fulfilling performance requirements and power consumption limits caused by the dark silicon issues. Within the same context, the research activities focus also on the definition of new runtime resource management policies for the optimization of the classical performance/power consumption trade-off in heterogeneous multi-core systems. The current research products are two SystemC simulation platforms for evaluating the various adaptive mechanisms ([SW.1] and [SW.4]), a Linux governor featuring the investigated resource management policies [SW.2] and the following list of publications: [IC.3], [JR.2], [JR.1], [WS.1], [JR.4], [JR.3], [IC.5], [IC.7], [IC.8], [IC.9], [IC.10], [JR.6], [IC.11], [IC.12], [JR.10], [IC.20], [IC.21], [WS.3] and [IC.25].

Fault simulation and analysis in SystemC transaction level specifications. The aim of this research is the definition of a methodological framework for the simulation of faults in SystemC transaction level models of embedded systems. The main issues of the research are 1) the modeling of the faults, since the considered models are described with a high level of abstraction, 2) the design of non-intrusive injection strategies for SystemC specifications and 3) the definition of approaches for the analysis of fault/error relationship and error propagation. A state-of-the-art simulation platform has been enhanced with the mechanisms defined in the research [SW.5], and the results have been presented in the following publications: [JR.7], [IC.26], [IC.35], [IC.38] and [IC.8].

Reliable Field Programmable Gate Array (FPGA) systems design. A methodology has been defined for implementing systems on FPGA with mitigation features for transient and permanent faults. The methodology is based on 1) a set of tunable reliability-oriented strategies defined by coupling traditional fault detection/tolerance techniques with the device dynamic reconfiguration property to achieve fault mitigation capabilities, and 2) an automated design space exploration framework for the hardening and implementation of the reliable FPGA-based system. The framework is devoted to the identification of the optimal selection and tuning of the hardening techniques in order to obtain a reliable implementation optimized with respect to resource utilization and performance metrics. Moreover, this research focuses also on the definition of fault injection and analysis strategies for FPGA-based systems. The research products are a software framework automating the design space exploration [SW.6], a prototype of the reliable FPGA-based system, and the following publications: [IC.15], [JR.8], [IC.22], [IC.24], [JR.13], [IC.31], [IC.32], [IC.33], [IC.34], [IC.37] and [IC.40].

Digital systems' design automation. Another area of interest covers other aspects of the design of computing systems, focusing on the design automation in terms of SystemC transaction level modeling and simulation of heterogeneous multiprocessor systems ([JR.12], [IC.23], [IC.28] and [IC.39]) and tools for FPGA systems' design ([IC.4], [JR.5], [WS.2], [IC.13] and [IC.27]).

METHODOLOGIES FOR THE PERSONALIZATION OF CONTEXT DEPENDENT DATA VIEWS

Dr. Miele's secondary research interests are related to the definition of methodologies for the personalization and the reduction of context dependent data views, belonging to the wider research area on contextual databases, called Context-ADDICT (`http://poseidon.elet.polimi.it/ca/`). In particular, the aim of this research is to study an extension of the Context-ADDICT data tailoring methodology by taking into account a set of *contextual preferences* specified by the user. On the basis of such preferences, describing which information the user is more interested in (and which not) in each specific context, the methodology imposes a relevance order among data and performs a reduction of the view in order to fit into the available memory of the mobile device. The research aims also at investigating approaches for the mining of preferences from the user's querying activities. The contribution started during the Ph.D. studies and continued during the post-doc period. The research products are a software framework supporting the methodology and the following publications: [IC.19], [JR.11] and [IC.36].

External Scientific Collaborations

List of external scientific collaborations (▶ ongoing collaborations).

- ▶ **University of California at Irvine** – In 2017, Dr. Miele started a collaboration with Prof. Nikil Dutt, Prof. Amir Rahmani (formerly affiliated at University of Turku, Finland) and Prof. Bruno Zatt dealing with the definition of runtime resource management policies for heterogeneous multi-core systems, with the specific focus on video processing applications.
- ▶ **University of Turku (Finland)** – Stemming from MEDIAN EU Cost Action activities, in 2014 Dr. Miele started a collaboration with Prof. Amir Rahmani and his team, on research activities dealing with the design of strategies for the reliability-aware runtime resource management for many-core systems in the dark silicon era. During this collaboration, Dr. Miele has contributed to the supervision of Mohammad Hashem Haghbayan (Ph.D. student at the University of Turku) in his research activities. In February 2015 and in February 2016, he visited the University of Turku for one week to work together; moreover, he hosted Mohammadhashem Haghbayan at Politecnico di Milano for a week in September 2015. At present, five papers and a book chapter have been published ([JR.2], [JR.4], [JR.3], [JR.6], [IC.7] and [BC.2]). Dr. Miele has also taught a Ph.D./master course on Heterogeneous System Architectures at the University of Turku in February 2016.
- ▶ **University of Piraeus (Greece)** – Within MEDIAN activities, Dr. Miele is collaborating with Prof. Mihalis Psarakis and his team on research dealing with the design of a self-healing FPGA-based processor and the definition of CAD tools for the implementation of reliable systems on FPGA. In January 2014, he visited the University of Piraeus for one week to finalize a paper presented in an international conference [IC.15]; an extended version of the paper will be submitted to a journal.
- **National University of Singapore (NUS)** – In 2013, Dr. Miele collaborated with Anup Kumar Das (Ph.D. student at NUS who attended a visiting period at Politecnico di Milano from May to July, 2013) on the definition of adaptive strategies for mitigating the aging in multi-/many-core architectures (publications: [IC.20] and [IC.18]).
- **Politecnico di Torino** – In 2006-2007, Dr. Miele collaborated with Prof. Massimo Violante and Prof. Maurizio Rebaudengo on a research devoted to the study of microprocessor reliability (publications: [JR.14], [IC.42]). In 2010, he also worked together with Prof. Violante for a study on strategies dealing with transient faults in FPGA systems (publications: [IC.33]).
- **ESA/ESTEC** – From 2008 to 2010, Dr. Miele collaborated with Dr. Giovanni Beltrame on a research devoted to the study of fault modeling and injection in SystemC transaction level specifications (publications: [IC.35], [IC.39], [IC.41]). Moreover, he contributed to a joint study on fault mitigation strategies for multi-FPGA platforms (publications: [IC.31]).

Professional Activities

National and International Research Projects

Dr. Miele contributed actively to the following research projects.

- **Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures (SAVE)**
  Type: FP7 STREP project
  Date: Sep. 2013 - Aug. 2016
  Local project leader: Prof. C. Bolchini
  Topic: The mission of SAVE (http://www.fp7-save.eu/) is to develop new hardware and software technologies for the implementation of self-adaptive computing systems suitable for the broad computing spectrum, exploiting heterogeneous resources, such as CPUs, GPUs and FPGAs available within the same architecture. The project vision is to provide solutions that facilitate the exploitation of specific islands of computation that offer interesting trade-offs in terms of energy/performance.
  Role: *Task 5.1 leader* and technical coordinator of the activities for the development of a virtual platform devoted to the validation of the investigated self-adaptive approaches. *Researcher* contributing to the activities of the other

tasks on the definition of self-adaptive policies for runtime resource management in heterogeneous multiprocessor systems. Contribution to the dissemination of the results by means of demos at conferences and project reviews, and co-author of papers regarding the project outcomes.

- **Smart multicore embedded systems: A holistic approach for the integration of multicore SoC and Embedded Software (SMECY)**
  TYPE: EU-ARTEMIS project
  DATE: Feb. 2010 - Jan. 2013
  LOCAL PROJECT LEADER: Prof. D. Sciuto
  TOPIC: SMECY project (http://www.smecy.eu/) envisions a rapid growth of recently emerged multi-core technologies in massively parallel computing environments which, due to improved performance, energy and cost properties, will extensively penetrate the embedded system industry in a few years. For this reason, the mission of the project is to develop new programming technologies enabling the exploitation of many-core architectures.
  ROLE: *Primary researcher* in the study of novel strategies and mechanisms enabling a dynamic support to fault management in many-core architectures, particularly focusing on ST/CEA P2012 platform. Support towards the definition of a strategy to dynamic applications' mapping in the same working scenario. Contribution to the dissemination of the results by preparing the demonstrations of the research products; co-author of publications presenting the project outcomes.

- **High reliability fault tolerant digital systems in nanometric technologies: characterization and design methodologies**
  TYPE: MIUR-PRIN 2008 project
  DATE: Mar. 2010 - Sept. 2012
  LOCAL PROJECT LEADER: Prof. C. Bolchini
  TOPIC: The goal of the project has been the definition of techniques to design and evaluate fault tolerant systems implemented using the System-on-Programmable-Chip (SoPC) paradigm, suitable for mission- and safety-critical application environments.
  ROLE: Contribution to the preparation of the project proposal. *Primary researcher* on the study of an automated design methodology for the hardening and implementation of reliable systems on SoPC against both transient and permanent faults. *Workpackage 3 leader* in the local unit for the application and experimental validation of the proposed hardening techniques in a set of case studies. Support for the research activities of a Ph.D. student in her work on the design of a reconfiguration controller architecture able to manage the recovery from faults. Contribution to the dissemination of the results as co-author of publications presenting the project outcomes.

- **Scalable low power embedded platforms (SCALOPES)**
  TYPE: EU-ARTEMIS project
  DATE: Jan. 2009 - Dec. 2010
  LOCAL PROJECT LEADER: Prof. D. Sciuto
  TOPIC: SCALOPES project (http://www.scalopes.eu/) focused on cross-domain technology and tool developments for multi-core architectures. In particular, the project investigated application and programming models, composability, dependability, reliability, predictable system design, resource management and tools supporting these new developments. Such developments have been driven by four different application domains: communication infrastructure, surveillance systems, smart mobile terminals and stationary video and entertainment systems.
  ROLE: *Primary researcher* in the activities of re-engineering and enhancement of a simulation platform for multiprocessor systems also to deal with reliability analysis of multiprocessor systems and reconfigurable network-on-chip modeling and simulation. Contribution to the dissemination of the results by preparing the demonstrations of the research products; as co-author of publications presenting the project outcomes.

EDITORIAL BOARDS

Dr. Miele is or has been a member of the Editorial Board of the following:

- **Guest co-Editor**, with Saqib Khursheed (Liverpool University, UK) and Martin Trefzer (University of York, UK), for a Special Issue of the IET Computers & Digital Techniques on "Defect and Fault Tolerance in VLSI and Nanotechnology Systems" (2018).
- **Guest co-Editor**, with Qiaoyan Yu (University of New Hampshire, USA) and Maria K. Michael (University of Cyprus, CY), for a Special Issue/Section of the IEEE Transactions on Emerging Topics in Computing on "Reliability-aware Design and Analysis Methods for Digital Systems: from Gate to System Level" (2016-2017).

CONFERENCE AND WORKSHOP ORGANIZATION

Program Chair and Organization Committees

Dr. Miele contributed to the organization of conferences with the following roles:

- **Topic Chair** of the Track A6 "Adaptive and Learning Systems" at Int. Conf. on Design Automation & Test in Europe (DATE), in 2019.
- **Topic Co-Chair** of the Track A6 "Reconfigurable and Robust Systems" at Int. Conf. on Design Automation & Test in Europe (DATE), in 2018.
- **Program Co-Chair** of the IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems, in 2017.
- **Program Co-Chair** of the IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems, in 2016.
- Publicity Chair for the IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems, from 2011 to 2015.
- Publicity Chair for the Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale in 2012 and 2013, held in conjunction with the European Test Symp.
- Publication Chair for the 1st Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms (ERDIAP) in 2011, held in conjunction with the 24th Int. Conf. on Architecture of Computing Systems.

Program Committee Membership

Dr. Miele is a member of the Program Committee of the following conferences:

- Int. Conf. on Design Automation & Test in Europe (DATE)
  - Track A6 "Adaptive and Learning Systems", in 2019.
  - Track A6 "Reconfigurable and Robust Systems", in 2018.
  - Track A6 "Reliable Aware Reconfigurable/Self-Adaptive Systems", in 2017.
  - Track A6 "Reliable and Reconfigurable Systems", in 2015.
- Int. Symp. on Applied Reconfigurable Computing (ARC) from 2014 to 2018.
- EUROMICRO Conf. on Digital System Design (DSD)
  - Special session on Dependability and Testing and Fault Tolerance in Digital Systems Design, from 2014 to 2018.
  - Special session on Fault Tolerance in Digital Systems Design, in 2013.
- IEEE Int. On-Line Testing Symposium (IOLTS), from 2013 to 2018.
- Reconfigurable Architectures Workshop (RAW) from 2016 to 2018.
- Int. Conf. on Field Programmable Logic and Applications (FPL), from 2011 to 2018.
- IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems (DFT), from 2012 to 2018.
- NASA/ESA Conf. on Adaptive Hardware and Systems (AHS), in 2015 and from 2017 to 2018.
- Symposium on Integrated Circuits and System Design (SBCCI) from 2016 to 2018.
- IEEE Latin-American Test Symposium (LATS), in 2017.
- Workshop on Reliability, Security and Quality (RESCUE) co-located with the IEEE European Test Symp., in 2017.
- IEEE Int. Conf. on ReConFigurable Computing and FPGAs (ReConFig), from 2013 to 2017.
- Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN), from 2012 to 2014.

REFEREE SERVICES

Dr. Miele served as an external reviewer for the following journals and conferences:

- ACM Computing Surveys, IEEE Transactions on Device and Materials Reliability, IEEE Transactions on Emerging Topics in Computing, ACM Transactions on Design Automation of Electronic Systems, ACM Transactions on

Architecture and Code Optimization, ACM Transactions on Reconfigurable Technology and Systems, IEEE Transactions on Computers, IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems II, IEEE Transactions on Evolutionary Computation, IEEE Micro, IEEE Embedded Systems Letters, Springer Computing, Springer Journal of Electronic Testing, Elsevier Journal of Parallel and Distributed Computing, Elsevier Future Generation Computer Systems, IET Computers & Digital Techniques.

- Design Automation Conf. (invited as Expert Reviewer in 2013), European Test Symp., Int. Conf. Hardware/software Codesign and System Synthesis. Int. Conf. on Computer-Aided Design.
- Int. Conf. on Design, Automation and Test in Europe, Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems, Int. Conf. on Field Programmable Logic and Applications, Int. On-Line Testing Symp., and EUROMICRO Conf. on Digital System Design, before joining the related committees.

MEMBERSHIP

- **MEDIAN** – In 2012, Dr. Miele joined the "Manufacturable and dependable multicore architectures at nanoscale" (MEDIAN) project, Cost Action no. IC1103 aiming at creating a European network of competence and experts on all dependability aspects of future digital systems development, promoting collaboration between industry and research. The project ended on December 2015.
- **HiPEAC** – Since 2012, Dr. Miele is affiliated member of the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC).
- **IEEE** – Dr. Miele is IEEE member since 2012.
- **ACM** – Dr. Miele is ACM member in 2017.

Awards

AW.1. Best Demo Award for "On the Automation of High Level Synthesis of Convolutional Neural Networks," [WS.2] *Proc. Reconfigurable Architecture Workshop* (RAW), 2016.

AW.2. Best Paper Award for "Reliability-Driven System-Level Synthesis of Embedded Systems," [IC.30] *Proc. 25th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems* (DFT), 2010.

AW.3. Co-author of the Best Student Paper Award (won by Chiara Sandionigi) for "A Reliable Reconfiguration Controller for Fault-Tolerant Embedded Systems on Multi-FPGA platforms," [IC.31] *Proc. 25th IEEE International Symposium on Defect and Fault-Tolerance in VLSI Systems* (DFT), 2010.

AW.4. Best Paper Candidate for "ReSP: A Non-Intrusive Transaction-Level Reflective MPSoC Simulation Platform for Design Space Exploration," [IC.39] *Proc. IEEE 13th Asia and South Pacific Design Automation Conference* (ASP-DAC), 2008.

Conference Attendance and Participation

- Int. Conf. on Design, Automation and Testing in Europe in 2018.
- Int. Symp. on Defect and Fault-Tolerance in VLSI Systems in 2017 as Program co-chair and for the presentation of [IC.3].
- Int. Conf. on Design, Automation and Testing in Europe in 2017.
- Int. Symp. on Defect and Fault-Tolerance in VLSI Systems in 2016 as Program co-chair.
- VLSI Test Symp. in 2016 for an invited talk "Lifetime reliability modeling and estimation in multi-core systems" in the special session "Managing lifetime in Manycore Systems".
- Int. Conf. on Design, Automation and Testing in Europe in 2016 for the presentation of [IC.8] and for chairing a session on "Anti-aging and Error protection using Checkpointing and DVFS".
- Int. Conf. on Computer Design in 2015 for the presentation of [IC.11] and for chairing a special session on "Data Mining for Computer Design".

- Int. Symp. on Defect and Fault-Tolerance in VLSI Systems in 2014 and co-located Joint MEDIAN-TRUDEVICE Open Forum for the presentation of [PS.2].
- HiPEAC Computing Systems Week, in 2014.
- Int. Conf. on Design, Automation and Testing in Europe in 2014 for the presentation of [IC.18] and for chairing a session on "Reliable Systems in the Age of Variability".
- Int. On-Line Testing Symp. in 2013.
- 8th HiPEAC Conf. in 2012 for the presentation of [PS.4].
- Int. Conf. on Field Programmable Logic and Applications in 2012.
- 1st Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale in 2012 for the presentation of [WS.3].
- European Test Symp. in 2012 for the presentation of [IC.24].
- Int. Conf. on Design, Automation and Testing in Europe in 2012 for the presentation of [IC.25] and of a demo of the tools proposed in [IC.30] and in [JR.13] at the University Booth (poster: [PS.5]).
- Int. Conf. on Field Programmable Logic and Applications in 2011 for the presentation of [IC.27].
- Great Lake Symposium on VLSI Systems (GLSVLSI) in 2011 for the presentation of [IC.29].
- Int. Conf. on Field Programmable Logic and Applications in 2010 for helping organizing as a Ph.D. student volunteer and for chairing a session on "Synthesis and Placement".
- European Test Symp. in 2010 for the presentation of [IC.33] and for the participation to the Ph.D. thesis contest (poster: [PS.6]).
- Int. Conf. on Design, Automation and Testing in Europe in 2010 where he presented a poster on his thesis in the Ph.D. forum (poster: [PS.7]).
- Great Lake Symp. on VLSI Systems in 2009 for the presentation of [IC.35].
- Int. Conf. on Extending Database Technology in 2009 for the presentation of [IC.36].
- Euromicro Conf. on Digital System Design in 2008 for the presentation of [IC.38].
- European Test Symp. in 2008 for the presentation of [PS.8].
- Int. Symp. on Defect and Fault-Tolerance in VLSI Systems in 2007 for the presentation of [IC.41] and [IC.40].
- Int. Symp. on Defect and Fault-Tolerance in VLSI Systems in 2005 for the presentation of [IC.43].
- Italian Symp. on Advanced Database Systems in 2004.

Invited talks

- "System-level lifetime reliability modeling and management in multi-core systems" at the New York University on September 29, 2016.
- "Lifetime reliability modeling and estimation in multi-core systems" in the embedded tutorial on "Managing lifetime in Manycore Systems" at the VLSI Test Symp. on April 27, 2016.
- "System-level Approaches for the Design of Reliable Embedded Systems" at the University of Piraeus, Greece, on February 12, 2014.

Quantitative Evaluations of Scientific Effort

PUBLICATIONS SUMMARY

- Refereed international journals ____ 14
- Editorial Contributions ____ 2
- Refereed international book chapters ____ 4
- Refereed international conferences ____ 44
- Refereed national conferences ____ 1
- Refereed international workshops ____ 4

FROM SCOPUS (HTTP://WWW.SCOPUS.COM) FOR THE PROFILE "ANTONIO MIELE" (QUERY DATE: 2018-06-05)

- Documents: 63
- Citations: 572 total citations by 478 documents
- h-index: 12

FROM GOOGLE SCHOLAR (HTTP://SCHOLAR.GOOGLE.IT/) FOR THE PROFILE "ANTONIO MIELE" (QUERY DATE: 2018-06-05)

- Citations (all): 838 h-index: 15; i10-index: 26
- Citations (since 2013): 616; h-index: 14; i10-index: 18

Complete publication list

REFEREED INTERNATIONAL JOURNALS

JR.1. C. Bolchini, S. Cherubin, G.C. Durelli, S. Libutti, A. MIELE, M.D. Santambrogio, "A Runtime Controller for OpenCL Applications on Heterogeneous System Architectures," *ACM SIGBED Reviews*, Vol. 15, no. 1, pp. 29–35, February 2018. (ISSN: 1551–3688).
[url: http://dx.doi.org/10.1145/3199610.3199614]

JR.2. M.H. Haghbayan, A. MIELE, A.M. Rahmani, P. Liljeberg, H. Tenhunen, "Performance/Reliability-aware Resource Management for Many-Cores in Dark Silicon Era," *IEEE Transactions on Computers*, Vol. 66, no. 9, pp. 1599–1612, September 2017. (ISSN: 0018–9340).
[url: http://dx.doi.org/10.1109/TC.2017.2691009]

JR.3. M.H. Haghbayan, A. MIELE, A.M. Rahmani, P. Liljeberg, A. Jantsch, C. Bolchini, H. Tenhunen, "Can Dark Silicon Be Exploited to Prolong System Lifetime?," *IEEE Design & Test*, Issue 2, pp. 51–59, April 2017. (ISSN: 2168–2356).
[url: http://dx.doi.org/10.1109/MDAT.2016.2630317]

JR.4. A.M. Rahmani, M.H. Haghbayan, A. MIELE, P. Liljeberg, A. Jantsch, H. Tenhunen, "Reliability-Aware Runtime Power Management for Many-Core Systems the in Dark Silicon Era," *IEEE Transactions on VLSI Systems*, Vol. 25, no. 2, pp. 427–440, February 2017. (ISSN: 1063–8210).
[url: http://dx.doi.org/10.1109/TVLSI.2016.2591798]

JR.5. M. Rabozzi, G.C. Durelli, A. MIELE, J. Lillis, M.D. Santambrogio, "Floorplanning Automation for Partial-Reconfigurable FPGAs via Feasible Placements Generation," *IEEE Transactions on VLSI Systems*, Vol. 25, no. 1, pp. 151–165, January 2017. (ISSN: 1063–8210).
[url: http://dx.doi.org/10.1109/TVLSI.2016.2562361]

JR.6. M.H. Haghbayan, A.M. Rahmani, A. MIELE, M. Fattah, J. Plosila, P. Liljeberg, H. Tenhunen, "A Power-Aware Approach for Online Test Scheduling in Many-core Architectures," *IEEE Transactions on Computers*, Vol. 65, no. 3, pp. 730–743, March 2016. (ISSN: 0018–9340).
[url: http://dx.doi.org/10.1109/TC.2015.2481411]

JR.7. A. MIELE, "A fault-injection methodology for the system-level dependability analysis of multiprocessor embedded systems," *Journal of Microprocessors and Microsystems - Embedded Hardware Design, Elsevier*, Vol. 38, no. 6, pp. 567–580, August 2014. (ISSN: 0141–9331)
[url: http://dx.doi.org/10.1016/j.micpro.2014.05.008]

JR.8. C. Bolchini, A. MIELE, C. Sandionigi, "Autonomous Fault-Tolerant Systems onto SRAM-based FPGA Platforms," *Journal of Electronic Testing: Theory and Applications, Springer*, Vol. 29, no. 6, pp. 779–793, December 2013. (ISSN: 0923–8174).
[url: http://dx.doi.org/10.1007/s10836-013-5418-4]

JR.9. C. Bolchini, A. MIELE, "Reliability-driven System-level Synthesis for Mixed-Critical Embedded Systems," *IEEE Transactions on Computers*. Vol. 62, No. 12, pp. 2489–2502, December 2013. (ISSN: 0018-9340).
[url: http://dx.doi.org/10.1109/TC.2012.226]

JR.10. C. Bolchini, M. Carminati, A. MIELE, "Self-Adaptive Fault Tolerance in Multi-/Many-Core Systems," *Journal of Electronic Testing: Theory and Applications, Springer*, Vol. 29, no. 2, pp. 159–175, April 2013. (ISSN: 0923–8174).
[url: http://dx.doi.org/10.1007/s10836-013-5367-y]

JR.11. A. MIELE, E. Quintarelli, E. Rabosio, L. Tanca, "A data-mining approach to preference-based data ranking founded on contextual information," *Information Systems, Elsevier*, Vol. 38, no. 4, pp. 524–544, June 2013. (ISSN: 0306-4379).
[url: http://dx.doi.org/10.1016/j.is.2012.12.002]

JR.12. A. MIELE, C. Pilato, D. Sciuto, "A Simulation-Based Framework for the Exploration of Mapping Solutions on Heterogeneous MPSoCs," *Int. Journal of Embedded and Real-Time Communication Systems, IGI Global*, Vol. 4, no. 1, pp 22–41, January–March 2013. (ISSN: 1947-3176).
[url: http://dx.doi.org/10.4018/jertcs.2013010102]

JR.13. C. Bolchini, A. MIELE, C. Sandionigi, "A novel design methodology for implementing reliability-aware systems on SRAM-based FPGAs," *IEEE Transactions on Computers*, Vol. 60, No. 12, pp. 1744–1758, December 2011. (ISSN: 0018-9340).
[url: http://dx.doi.org/10.1109/TC.2010.281]

JR.14. C. Bolchini, A. MIELE, M. Rebaudengo, F. Salice, D. Sciuto, L. Sterpone, M. Violante, "Software and Hardware Techniques for SEU Detection in IP Processors," *Journal of Electronic Testing: Theory and Applications, Springer*, Vol. 24, no. 1-3, pp. 35–44, June 2008. (ISSN: 0923–8174).
[url: http://dx.doi.org/10.1007/s10836-007-5028-0]

EDITORIAL CONTRIBUTIONS

ED.1. R. Shafik, Q. Yu, S. Khursheed and A. MIELE, "Welcome Message," *Proceedings of 2017 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2017, pp. iii. (ISBN: 978-1-5386-0362-8).
[url: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8244425]

ED.2. O. Khan, M.K. Michael, A. MIELE and Q. Yu, "Foreword," *Proceedings of 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2016, pp. iii. (ISBN: 978-1-5090-3623-3).
[url: http://dx.doi.org/10.1109/DFT.2016.7684056]

REFEREED CHAPTERS IN INTERNATIONAL BOOKS

IB.1. C. Bolchini, M.K. Michael, A. MIELE, S. Neophytou, "Dependability Threats," in *M. Ottavi, D. Gizopoulos, and S. Pontarelli (eds.) "Dependable Multicore Architectures at Nanoscale"*, pp. 37-92 Springer, 2018 (ISBN: 978-3-319-54421-2).
[url: http://www.springer.com/gp/book/9783319544212]

IB.2. M.H. Haghbayan, A.M. Rahmani, A. MIELE, P. Liljeberg, H. Tenhunen, "Online Software-Based Self-Testing in the Dark Silicon Era," in *A.M. Rahmani, P. Liljeberg, A. Hemani, A. Jantsch, and H. Tenhunen (eds.) "The Dark Side of Silicon - Energy Efficient Computing in the Dark Silicon Era"*, pp. 259–287, Springer, 2017 (ISBN: 978-3-319-31596-6).
[url: http://www.springer.com/gb/book/9783319315942]

IB.3. V. Rana, F. Bruschi, A. MIELE, M.D. Santambrogio, D. Sciuto, "Design Methodologies for Reconfigurable NoC-Based Embedded Systems," in *Pierre-Emmanuel Gaillardon (eds.) "Reconfigurable Logic: Architecture, Tools, and Applications"*, pp. 185–213, CRC Press, 2015 (ISBN: 978-1-4822-6218-6).
[url: https://www.crcpress.com/Reconfigurable-Logic-Architecture-Tools-and-Applications/Gaillardon/9781482262186]

IB.4. G. Agosta, M. Cartron, A. MIELE, "Fault Tolerance," in *M. Torquati, K. Bertels, S. Karlsson, F. Pacull (eds.) "Smart Multicore Embedded Systems"*, pp. 79–99, Springer, 2014 (ISBN: 978-1-4614-8799-9).
[url: http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4614-8799-9]

REFEREED INTERNATIONAL CONFERENCES

IC.1. R. Pinciroli, A. Bobbio, C. Bolchini, D. Cerotti, M. Gribaudo, A. MIELE, K. Trivedi, "Epistemic Uncertainty Propagation in a Weibull Environment for a Two-Core System-on-Chip," *Proc. Int. Conf. on System Reliability and Safety* (ICSRS), 2017, pp. 516–520.
[url: https://doi.org/10.1109/ICSRS.2017.8272875]

IC.2. A. Bobbio, C. Bolchini, D. Cerotti, M. Gribaudo, A. MIELE, "Scalable analytical model of the reliability of multi-core systems-on-chip by interacting Markovian agents," *Proc. EAI Int. Conf. on Performance Evaluation Methodologies and Tools* (VALUETOOLS), 2017, pp.1–9.

IC.3. C. Bolchini, A. Baldassari, A. MIELE, "A Dynamic Reliability Management Framework for Heterogeneous Multicore Systems," *Proc. IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems* (DFT), 2017, pp. 1–6.
[url: https://doi.org/10.1109/DFT.2017.8244440]

IC.4. M. Rabozzi, G. Natale, B. Festa, A.MIELE, M.D. Santambrogio, "Optimizing Streaming Stencil Time-step Designs via FPGA Floorplanning," *Proc. Conf. on Field Programmable Login and Applications* (FPL), 2017, pp. 1–4.
[url: https://doi.org/10.23919/FPL.2017.8056764]

IC.5. M. Pogliani, G.C. Durelli, A. MIELE, T. Becker, P. Sanders, M.D. Santambrogio, C. Bolchini, "Quality of Service Driven Runtime Resource Allocation in Reconfigurable HPC Architectures," *Proc. Conf. on Embedded and Ubiquitous Computing* (EUC), 2016, pp. 16–23.
[url: http://doi.org/10.1109/CSE-EUC-DCABES.2016.156]

IC.6. A. MIELE, "Lifetime reliability modeling and estimation in multi-core systems," *Proc. on VLSI Test Symp.* (VTS), 2016, pp. 1.
[url: http://dx.doi.org/10.1109/VTS.2016.7477315]

IC.7. M. Haghbayan, A. MIELE, A. Rahmani, J. Plosila, H. Tenhunen, "A Lifetime-Aware Runtime Mapping Approach for Many-core Systems in the Dark Silicon Era," *Proc. Conf. on Design, Automation and Testing in Europe* (DATE), 2016, pp. 854–857.
[url: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=7459428]

IC.8. C. Bolchini, L. Cassano, A. MIELE, "Lifetime-aware Load Distribution Policies in Multi-core Systems: An In-depth Analysis," *Proc. Conf. on Design, Automation and Testing in Europe* (DATE), 2016, pp. 804–809.
[url: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=7459416]

IC.9. E. Del Sozzo, G.C. Durelli, E.M.G. Trainiti, A. MIELE, M.D. Santambrogio, C. Bolchini, "Workload-aware Power Optimization Strategy for Asymmetric Multiprocessors," *Proc. Conf. on Design, Automation and Testing in Europe* (DATE), 2016, pp. 531–534.
[url: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=7459367]

IC.10. E.M.G. Trainiti, G.C. Durelli, A. MIELE, C. Bolchini, M.D. Santambrogio, "A Self-Adaptive Approach to Efficiently Manage Energy and Performance in Tomorrow's Heterogeneous Computing Systems," *Proc. Conf. on Design, Automation and Testing in Europe* (DATE), 2016, pp. 906–911.
[url: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=7459437]

IC.11. C. Bolchini, G.C. Durelli, A. MIELE, G. Pallotta, M.D. Santambrogio, "An orchestrated approach to efficiently manage resources in heterogeneous system architectures," *Proc. IEEE Int. Conf. on Computer Design* (ICCD), 2015, pp. 221–228.
[url: http://dx.doi.org/10.1109/ICCD.2015.7357104]

IC.12. A. MIELE, G.C. Durelli, M.D. Santambrogio, C. Bolchini, "A System-Level Simulation Framework for Evaluating Resource Management Policies for Heterogeneous System Architectures," *Proc. IEEE Int. Symp. on Digital Systems Design* (DSD), 2015, pp. 637–644.
[url: http://dx.doi.org/10.1109/DSD.2015.99]

IC.13. M. Rabozzi, A. MIELE, M.D. Santambrogio, "Floorplanning for Partially-Reconfigurable FPGAs via Feasible Placements Detection," *Proc. IEEE Int. Symp. on Field-Programmable Custom Computing Machines* (FCCM), 2015, pp. 252–255.
[url: http://dx.doi.org/10.1109/FCCM.2015.16]

IC.14. C. Bolchini, M. Carminati, M. Gribaudo, A. MIELE, "A lightweight and open-source framework for the lifetime estimation of multicore systems," *Proc. IEEE Int. Conf. on Computer Design* (ICCD), 2014, pp. 166–172.
[url: http://dx.doi.org/10.1109/ICCD.2014.6974677]

IC.15. M. Psarakis, A. Vavousis, C. Bolchini, A. MIELE, "Design and implementation of a Self-Healing Processor on SRAM-based FPGAs," *Proc. IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems* (DFT), 2014, pp. 165–170.
[url: http://dx.doi.org/10.1109/DFT.2014.6962076]

IC.16. G.C. Durelli, M. Pogliani, A. MIELE, C. Plessl, H. Riebler, M.D. Santambrogio, G. Vaz, C. Bolchini, "Runtime Resource Management in Heterogeneous System Architectures: The SAVE Approach," *Proc. Int. Symp. on Parallel and Distributed Processing with Applications* (ISPA), 2014, pp. 142–149.
[url: https://doi.org/10.1109/ISPA.2014.27]

IC.17. G.C. Durelli, M. Coppola, K. Djafarian, G. Kornaros, A. MIELE, M. Paolino, O. Pell, C. Plessl, M.D. Santambrogio, C. Bolchini, "SAVE: Towards efficient resource management in heterogeneous system architectures," *Proc. Int. Symp. on Applied Reconfigurable Computing* (ARC), 2014, pp. 337–344.
[url: http://dx.doi.org/10.1007/978-3-319-05960-0_38]

IC.18. C. Bolchini, A. MIELE, A. Das, A. Kumar, B. Veeravalli, "Combined DVFS and Mapping Exploration for Lifetime and Soft-Error Susceptibility Improvement in MPSoCs," *Proc. Conf. on Design, Automation and Testing in Europe* (DATE), 2014, pp. 1–6.
[url: http://dx.doi.org/10.7873/DATE.2014.074]

IC.19. A. MIELE, E. Quintarelli, E. Rabosio, L. Tanca, "ADaPT: Automatic Data Personalization Based on Contextual Preferences," *Proc. IEEE Int. Conf. on Data Engineering* (ICDE), 2014, pp. 1234–1237.
[url: http://dx.doi.org/10.1109/ICDE.2014.6816749]

IC.20. C. Bolchini, M. Carminati, A. MIELE, A. Das, A. Kumar, B. Veeravalli, "Run-Time Mapping for Reliable Many-Cores Based on Energy/Performance Trade-offs," *Proc. IEEE Int. Symp. on Defect and Fault-Tolerance in VLSI and Nanotechnology Systems* (DFT), 2013, pp. 58–64.
[url: http://dx.doi.org/10.1109/DFT.2013.6653583]

IC.21. C. Bolchini, M. Carminati, A. MIELE, E. Quintarelli, "A Framework to Model Self-Adaptive Computing Systems," *Proc. NASA/ESA Conf. on Adaptive Hardware and Systems* (AHS), 2013, pp. 71–78.
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PS.2. C. Bolchini, A. MIELE, "System-level Approaches for the Design of Reliable Embedded Systems," *Joint MEDIAN-TRUDEVICE Open Forum*, 2014.

PS.3. C. Bolchini, M. Carminati, A. MIELE, "Improving Reliability, Lifetime and Energy Consumption of Multi/Manycore Systems," *1st Int. Training School on Manufacturable and Dependable Multi-core Architectures at Nanoscale* (MEDIAN), 2013.

PS.4. C. Bolchini, M. Carminati, A. MIELE, "Self-Adaptive Fault Tolerance in Multi-/Many-Core Systems," *Int. Conf. on High-Performance and Embedded Architectures and Compilers* (HiPEAC), 2013.

PS.5. C. Bolchini, A. MIELE, "Reliability-Aware Embedded Systems Design Suite," *University Booth at Conf. on Design, Automation and Testing in Europe* (DATE), 2012.

PS.6. A. MIELE, "A Methodology for the Design and the Analysis of Reliable Embedded Systems," *TTTC's E. J. McCluskey Doctoral Thesis Award Contest at European Test Symp.* (ETS), 2010.

PS.7. A. MIELE, "A Methodology for the Design and the Analysis of Reliable Embedded Systems," *Ph.D. Forum at Conf. on Design, Automation and Testing in Europe* (DATE), 2010.

PS.8. C. Bolchini, A. MIELE, D. Sciuto, "Fault Models and Injection Strategies for a Reflective Simulation Platform," *Proc. IEEE European Test Symp.* (ETS), 2008.

Software tools

The list of publicly available softwares developed in relation with the research activities.

SW.1. **SAVE Virtual Platform (2015)** is a system-level functional simulator for heterogeneous multi-core systems developed in SystemC and TLM. The platform is devoted to the design and the analysis of run-time resource management policies and dynamic application mapping. The tool has been developed within the activities of SAVE project by Dr. Miele and G. Durelli (research assistant at Politecnico di Milano), and is available on request at https://trac.ws.dei.polimi.it/D4De.

SW.2. **SAVE Orchestrator (2015)** is a runtime resource manager implemented in a Linux-based machine. The governor features a set of policies for the accurate distribution of the workload on the processing units and the tuning of architectural knobs (such as the dynamic voltage/frequency scaling) in a heterogeneous multi-core system. The governor has been developed within the activities of SAVE project by a team of Ph.D. students and researches at Politecnico di Milano, and is available at https://bitbucket.org/necst/save-orchestrator-release/downloads/. An alternative version of the manager, presented in [JR.1], is available at https://bitbucket.org/necst/opencl-cgroups-library-release.

SW.3. **Caliper (2014)** is a tool based on Monte Carlo simulations for the estimation of the lifetime reliability of heterogeneous multi-core system under a variable workload and tolerating multiple failures. The tool, developed by Dr. Miele and M. Carminati (Ph.D. student at Politecnico di Milano), is available at https://github.com/D4De/caliper.

SW.4. **ReDSE (2010-2014)** is a suite of software tools for the reliability-driven system-level design of multi-core systems. In particular the suite contains i) tools for the design space exploration aimed at optimizing the hardening techniques application considering both transient faults and aging effects, and ii) functional simulators for the design and validation of reliability-driven runtime resource management policies. The tool suite, developed by Dr. Miele, is available on request at https://trac.ws.dei.polimi.it/D4De.

SW.5. **ReSP (2010)** is a simulation platform for heterogeneous multiprocessor systems based on Instruction Set Simulators and implemented in SystemC and TLM. Within the activities of SCALOPES project, Dr. Miele contributed to the re-engineering and enhancement of the current version of the tool starting from a preliminary implementation to support advanced features and modules (such as reconfigurable HW modules and NoC infrastructures). The development team was composed of 4 researchers. The tool is publicly downloadable at https://code.google.com/p/resp-sim.

SW.6. **R4R (2009-2011)** is a suite of software tools for the analysis and the design of fault tolerant systems on FPGA platforms. It contains i) tools for the design space exploration aimed at optimizing the hardening techniques application, ii) a fault injection framework for emulating soft-errors in FPGA boards, iii) a tool for the FPGA floorplanning, and iv) utility tools for the visualization of the system architecture and automatic generation of the HDL code. The tool suite has been developed by Dr. Miele and Prof. C. Bolchini partially within the activities of a MIUR-PRIN project, and is available on request at https://trac.ws.dei.polimi.it/D4De.

Milan, June 5, 2018

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