Abstract—Future switching and interconnection fabrics inside switching equipment, high-performance computers and data-centers will require more throughput and more energy efficiency. Optical technology provides many opportunities of improvement of both features compared to electronic counterparts. This work defines a procedure to design the architecture of the optical multistage switching networks. Modularity of the implementation is the primary concern, allowing for the construction of a generic-size fabric by the simple cascading of multiple stage-modules. In this paper we show in details the application of the approach to a family of banyan networks. The designed architecture can be exploited for various implementation technologies, as, for instance, integrated optics with micro-ring resonators, free-space optics with 2-D MEMS, networks on chip.

I. INTRODUCTION

Nowadays interconnection is the new frontier for optical communications. Optical interconnection is the conventional term that indicates the usage of photonic systems to interconnect several optoelectronic high-speed transmitters and receivers located at short distance from one another. “Short” means in general subsystems within a system, e.g.: rack-to-rack (e.g. inside data-center, supercomputing or top-line switching facilities), shelf-to-shelf (e.g. backplane of a rack of servers or pc blades or card modules), board-to-board (e.g. the bus inside a computer), chip-to-chip (e.g. over a printed-circuit board), on-chip (e.g. interconnecting the cores of a multicore microprocessor). For all these applications, light offers strong advantages over current of electrons as means to propagate information. These are: extremely large bandwidth; attenuation that deos not increase with frequency; absence of electromagnetic interference; low cost, high robustness and small footprint of the transmission media; low power consumption; etc.

In the context of data-centers, for instance, optical interconnections proved to be an effective solution, not only for data-center remote connection [1], [2] but also for the intra-data-center infrastructure [3].

At the other extreme in the scale of interconnection distance, silicon technology evolution recently allowed the development of the System-on-Chip (SoC) concept, in which tens of subsystems (CPU, memory, I/O interfaces, etc.) may be integrated on a single chip. A full-functionality network (Network-on-Chip - NoC) has to be implemented to manage data exchanges between these subsystems [4], [5]. Thanks to the advantages mentioned above, silicon waveguides and photonics can guarantee good scalability in transmission bitrate, number of nodes and power consumption.

The optical implementation of multistage switching networks has been widely studied by researchers. Several transmission media (including fiber, waveguide and free-space optics) have been investigated, to match various types of components (e.g. MEMS, micro-ring resonators, directional couplers, etc.) for implementing the switching elements. There are recent works proposing multistage-network design techniques which are interesting but rather generic on how to physically interconnect the stages and the switching elements [6]. Other studies propose solutions not compatible with an integrated-optics implementation [7]. Some papers appeared in 2008 [8] present architectures developed for MEMS switching elements, which can however be easily extended to wave-guided systems. More recent studies (2009) deal with multistage network architectures exploiting waveguides and micro-ring resonators [9]. Most of these papers focus on networks of specific size, without caring too much about the scalability of the proposed architectures. An example of scalability study of MEMS matrices is presented in [10]. In this work, as in the others cited so far, the proposed architecture is a direct implementation of classical switching networks (e.g. Benes).

Novel optically-oriented architectures for multi-stage networks have been introduced in the 80’s and 90’s [11]–[13], exploiting directional couplers as switching elements. These works focused on the topology and are not very specific on the interconnection layout. A first paper investigating the modularity of an integrated-optics architecture based on directional couplers [14] appears in 2000: in the work a recursive design technique is proposed. In 2001, another similar study [15] reports a recursive technique to design the stages of a multistage network, independently on the topology of the switching elements; little attention is however dedicated to the interconnection of the stages. Meanwhile, in [16] an analogous approach is adopted to design MEMS-based stages.

In this work we would like to propose a design technique for optical multistage switching networks. Our contribution appears innovative compared to past literature as it aims at: being usable in both integrated-optics and free-space architectures, and thus compatible with several switching-element technologies (e.g. MEMS and micro-ring resonators); being scalable to networks of any size and based on a vast class of topologies (e.g. all the banyan networks); taking care of...
both stage internal architecture and interconnections between stages, allowing for a highly-modular implementation of the network; display a low complexity but be based on a systematic analysis of the properties of the architectures. We will refer to a planar implementation, in which optical signals propagate (in waveguide or free-space) over a plane parallel to the substrate of the network, over which the elements to switch or steer beams are fabricated.

II. MULTISTAGE-NETWORK BASIC DEFINITIONS AND DECOMPOSITION

As well known from the switching theory [17], a multistage network is composed by elementary switching elements (SEs) organized as a sequence of switching-element stages (SESs), interconnected by interstage links. Here only networks with $2 \times 2$ switching elements (SEs) are considered, each element having only two possible states: bar and cross. The links between two adjacent switching stages form an interstage-link stage (ILS). We will consider only networks with $N$ inlets and outlets $(N \times N)$ with $S$ switching stages, numbered from 1 to $S$ and $N/2$ SEs per stage. The number of interstage-link stages is $S−1$, each one numbered after its upstream switching stage (see Fig. 1).

![Figure 1: General scheme of a multistage network](image)

The routing, blocking and reachability properties of a multistage network depend on the number of SESs and the connection patterns built in the ILSs. Both SESs and ILSs perform permutations. In general, an $N \times N$ stage performs a permutation $\alpha = \eta(i)$ by mapping its inputs $i \in \{0, N−1\}$ one-to-one over its outputs $o$, with $0 \leq o \leq N−1$. The identity permutation $I$ occurs when $\eta(i) = i \ \forall i$. The permutation performed by two adjacent stages is the cascade of the permutations of each single stage, i.e. $\eta_1 \eta_2 = \eta_2 [\eta_1(i)]$, if $\eta_1$ and $\eta_2$ are the two individual permutations.

An SES performs a switching permutation $\pi$ which changes over time according to the network state, while an ILS performs a fixed interstage permutation $\mu$. Thus the overall permutation of a multistage network can be written as

$$\pi_S \mu_S \pi_{S−1} \mu_{S−1} \pi_{S−2} \mu_{S−2} \cdots \pi_{1} \mu_{1} \pi_{0}.$$

The switching theory has identified a number of interstage permutations that can be effectively used as basic building blocks in the construction of multistage networks. These networks are classified on the basis of the type of $\mu$ they adopt in their ILSs. One of the basic classes of ILS [17] is the set of the bit-exchanging permutations. In this paper we will deal only with this ILS type, though the method we describe can be applied also to other ILS permutations. The well-known banyan networks are all based on bit-exchanging permutation ILSs.

In bit-exchanging permutations, $N$ is an integer power of 2 $(N = 2^n)$ and thus inlets (outlets) of a generic stage are identified by a binary address of type: $a = a_{n−1}a_{n−2} \cdots a_0 \ (a_j \in [0, 1])$, where $a_{n−1}$ is the most significant bit. The inlet of stage $s$ with address $i_{n−1}i_{n−2} \cdots i_0$ is connected to the outlet of $s$ with address $a_{n−1}a_{n−2} \cdots a_0 = f(i_{n−1}i_{n−2} \cdots i_0)$, where $f$ indicates an operator that scrambles the bits (i.e. exchanges the position of one or more bit) in a prefixed order.

For the construction of the different banyan network topologies the following bit-exchanging permutations are defined [17]:

- $\sigma_h(i_{n−1} \cdots i_0) = i_{n−1}i_{n−1}i_{n−3}i_{n−3}i_0 \cdots i_0i_h$
- $\sigma^{-1}_h(i_{n−1} \cdots i_0) = i_{n−1}i_{n−1}i_{n−3}i_{n−3}i_0 \cdots i_0i_h$
- $\beta_h(i_{n−1} \cdots i_0) = i_{n−1}i_{n−1}i_{n−3}i_{n−3}i_0 \cdots i_0i_h$
- $\delta(h_{n−1} \cdots i_0) = i_{h2}i_{h2}i_{n−1}i_{n−1}i_0$
- $\rho(i_{n−1} \cdots i_0) = i_{h1}i_{h1}i_{n−2}i_{n−2}i_0$
- $I(i_{n−1} \cdots i_0) = i_{n−1}i_{n−2} \cdots i_0$

where $(0 \leq h \leq n−1)$.

Permutations $\sigma_h$ and $\sigma^{-1}_h$ are called $h$-shuffle and $h$-unshuffle, respectively, as they are one the mirror of the other. If $h = n−1$, the two permutations are named perfect shuffle ($\sigma$) and perfect unshuffle ($\sigma^{-1}$). The $\beta$ permutation is called butterfly, $\delta$ and the $\rho$ are known as bit-switch and bit-reversal, respectively, while $I$ is the identity.

The family of bit-exchanging permutations can be further divided into two classes, according to the property of preserving or not preserving the purity of the inlet in the input-output mapping. Formally, if $a_{n−1}a_{n−2} \cdots a_0 = f(i_{n−1}i_{n−2} \cdots i_0)$ is the permutation, then:

- the permutation is parity-preserving if $a_0 = i_0 \ \forall i$;
- the permutation is non parity-preserving otherwise.

**Observation 1.** Bit-switch and identity permutations are parity-preserving, while shuffle, unshuffle, butterfly and bit-reversal are non parity-preserving.

In this paper we restrict the illustration of our method only to bit-exchanging permutations that are not parity-preserving (for short, named NPBP in the following), leaving the extension to the parity-preserving permutations to future publications.

Let us now introduce a final concept we need for the following discussion. We define a superstage (SuS) as the set composed by the cascade of a switching stage and the following adjacent interstage-link stage. In a multistage network of $S$ stages, in which $\pi_s (\mu_s)$ is the permutation of the generic
SES (ILS), the SuS permutation is given by
\[
\omega_N(s) = \begin{cases} 
\pi_{s, \mu} & \text{for } 1 \leq s \leq S - 1 \\
\pi_{s} & \text{for } s = S 
\end{cases}
\]

In order to describe a SuS, and without loss of generality, in the following we will assume that the SES permutation is the identity: \( \pi_s = I \). This is equivalent to consider all the switching elements in the bar state and it implies that all connections between SuS inlets and outlets are arranged as the links of the ILS. This artifice will be useful to simplify the explanations of the optical SuS in Sec. III.

Any multistage network can be decomposed in a cascade of SuSs, as shown in Fig. 2 for the case of an \( 8 \times 8 \) network with shuffle ILSs. Dually, we can create a multistage network by cascading SuSs. The cascadability of SuSs is made possible by shuffle ILSs. Dually, we can create a multistage network by cascading SuSs. The cascadability of SuSs is made possible by shuffle ILSs.

A useful tool to represent the SuS layout and its internal architecture is provided by the substrate grid represented in Fig. 4 (in the case \( N = 8 \)). The grid has size \( N \times N \), with columns and rows numbered from 1 to \( N \); the SuS is inscribed in this grid: due to the “I” shape, the lower-right quarter of the grid is unused. Row height and column width are equal and an element of the grid is called base unit. Three sample optical paths are shown in the Fig. 4a in order to give a quick idea of the internal structure of the SuS. Optical paths are composed only of vertical and horizontal segments joined by 90-degrees turns. Each element of the grid can be only of a finite number of types: horizontal straight segment (e.g. \( (1, 1) \) in the grid), vertical straight segment (e.g. \( (4, 4) \)), left turn\(^1\) (e.g. \( (7, 4) \)), right turn (e.g. \( (2, 8) \)), turn pair (e.g. \( (2, 4) \)), path crossing intersection (at 90º) (e.g. \( (2, 6) \)). The final type is a path-crossing intersection which hosts an optical 2 × 2 switching device (that is supposed to have the two states: cross and bar) (e.g. \( (1, 4) \)). In this work we do not consider wavelength division multiplexing: all signals are assumed to be at the same wavelength. Therefore the following conflict-prevention rule must be enforced: no element of the substrate grid can be occupied by two co-propagating optical paths.

We are going now to further detail SuS planning.

A. Inlet/outlet placement

Inlets and outlets of the optical SuS are positioned as represented in Fig. 4b. They are partitioned according to their

\(^1\)Turns are implemented by fixed mirrors in case of free-space optics and by bended waveguides in integrated optics.
parity and the distance between two adjacent inlets (outlets) is equal to the base unit. Even inlets, starting from inlet 0, are placed at the edge of the top row, from column $N/2$ to column 1; odd inlets, starting from inlet 1, are placed at the edge of the leftmost column, from row 1 to row $N/2$. The inlets have been numbered so that inlets 0 and $N-1$ are symmetrical relative to the main diagonal of the grid (see Fig. 4b). Outlets are placed in positions which match the positions of the inlets of the next SuS: odd outlets are located at the edge of column $N/2$, from row $N/2 + 1$ to row $N$; even outlets are at the edge of row $N/2$, from column $N$ to column $N/2 + 1$. Fig. 5 shows an example of a multistage network built by cascading three $8 \times 8$ SuSs.

Figure 5: Three-stage network with corresponding SuS implementation

B. Optical paths

We require that optical paths have to connect inlets to outlets along the shortest possible way and with the minimum number of turns. In fact by reducing the number of path turns we reduce the loss due to bending or reflection on non-ideal mirrors.

As shown in Fig. 6, when an even (horizontal) inlet is connected to an odd (vertical) outlet, the simplest possible path is composed only by two segments and one turn. The same applies to a connection between an odd (vertical) inlet and an even (horizontal) outlet. These are named unique paths since one single path exists, once the inlet-outlet pair $[i,o]$ to be connected is selected. If the inlet $i$ is even (odd), the first segment of the path will lay on the column (row) $c_i$ ($r_i$) and the second segment will lay on the row (column) $r_o$ ($c_o$).

When the inlet and the outlet to be connected have the same parity (i.e. are both odd or even), the simplest possible path is composed of three segments and two turns. In this case, however, there are multiple possible paths, all with the same length, as visible in Fig. 6. Therefore there is a degree of freedom in the selection of the path: we introduce then the name free paths. If the source inlet is even (odd) the free path is described by $(c_i, r_t, c_o)$ ($r_i, c_t, r_o$); $r_t$ ($1 \leq r_t \leq N/2$) and $c_t$ ($1 \leq c_t \leq N/2$) indicate the row and column, respectively, selected for placing the central segment. The paths are named horizontal or vertical according to the orientation of their longest segment, which is the first one for the unique paths and the middle one for the free paths.

Observation 2. All SuS bit-exchanging permutations have at least two free paths implementing the links $[0,0]$ and $[N-1,N-1]$.

In fact the two links are obviously parity preserving, and thus correspond to free paths.

C. Switching elements

As stated above, the path-crossing intersection of inlet pairs $2k$ and $2k+1$ hosts an optical SE: therefore the paths of that inlet pairs must intersect. It can be proven that it is always possible to configure the paths in a way such that the pair of paths intersects at least once. This intersection always occurs in the element $(i,N/2-i+1)$ of the substrate grid: in this element we can locate the optical SE. Fig. 7 shows an $8 \times 8$ perfect-unshuffle optical SuS.

Figure 7: Optical SuS: $8 \times 8$ perfect-unshuffle

D. Last stage

In a multistage network decomposed in SuSs, the last SuS simply implements the identity permutation (see Fig. 2). This terminal SuS can be more effectively designed according to an ad-hoc procedure, derogating from the one described above for the other SuSs. In fact the terminal SuS can be simplified, since there is no need to connect it to a further stage. Fig. 8 represents the terminal SuS.

IV. DESIGN PROCEDURE OF OPTICAL MULTISTAGE NETWORKS

Based on the discussion above, the design procedure of the architecture of an optical multistage networks can be summarized as follows:

1) consider the multistage network represented as a sequence of SESs and ILSs (“classical” representation);
2) decompose the network in SuSs;
3) iteratively define the configuration of each optical SuS by means of the SuS design algorithm;
4) connect all the SuS modules to obtain the full network.

We report here two examples of application: a $16 \times 16$ switching-banyan (blocking) network (Fig. 9) and a $16 \times 16$ Benes (rearrangeable) network (Fig. 10). The optical architectures are represented rotated by 45° counter-clockwise compared to the convention adopted in the previous figures. Network inlets are on the left edge and outlets on the right edge of the networks.

**Figure 8: Terminal SuS**

**Figure 9: 16 × 16 SW-banyan network**

**Figure 10: 16 × 16 Benes network**

**V. CONCLUSIONS**

We have defined a systematic technique to design optical multistage networks based on “classical” switching architectures, known from the switching theory. Our approach lets us precisely specify the structure of the switching-stage modules and how to interconnect them, and it is compatible with both integrated and free-space optics and several photonic-device technologies. All the results reported in this paper, regarding the SuS architecture construction, are backed by a set of theorems based on the switching-network theory that have been formally proved. In particular, we have demonstrated that exploiting a layout of the type represented in Fig. 7 is a sufficient condition to implement any possible NPBP-based network. Theorems and proofs will be presented in a full paper. In this paper we have shown the application of the method to the family of banyan networks based on NPBP permutations. However the technique can be extended to other families of interstage permutations.

**REFERENCES**