Course Introduction

Marco D. Santambrogio
marco.santambrogio@polimi.it
FPGA-based System Design

Course Objectives

• Have each students to design an FPGA-based system
  – SoC
  – HPC
  – HW accelerators
  – etc..

• Envision where/how/why to use FPGAs in students’ research
FPGA-based System Design

Topics

• VHDL (5h)
• [Tools/VM+] IP-Cores synthesis (5h)
• IP-Cores simulation (2h)
• Design of an FPGA SoC using EDK (3h)
• Reconfiguration (Partial, Dynamic, etc…) (3h)
• Projects assignments (2h)
A possible agenda

- **VHDL (5h)**
  - 18/3 @ 2pm (2.5h) & 19/3 @ 10am (2.5h)
- **Tools/VM+IP-Cores synthesis (5h)**
  - 25/3 @ 2pm (3h) & 26/3 @ 10am (2h)
- **IP-Cores simulation (2h)**
  - 28/3 @ 9.30am (2h)
- **Design of an FPGA SoC using EDK (3h)**
  - 1/4 @ 2pm (3h)
- **Reconfiguration (Partial, Dynamic, etc…) (3h)**
  - 2/4 @ 10am (3h)
- **Projects assignments (2h)**
  - 4/4 @ 9am (2h)
Projects

• Self-assigned projects
  – Systems design proposed by the students

• Research projects
  – Research projects identified by the instructor
  – Work on both theoretical and technical/engineering aspects will be carried on…
    • A good starting point, if interested, to discuss/evaluate a possible publication
Tools and FPGAs

- Xilinx FPGA (e.g. V5 and Zynq)
- Xilinx tools

Obviously, Xilinx is not the only FPGA vendors, but it is the one that we are using in the lab with a sufficient amount of boards that can be shared/used by the students.
I need to know you...
Exams

• When: 17/4 @ 9am (3h) && @ 2pm (3h)
• What: Present to the rest of the class the project
Exams

- When: 17/4 @ 9am (3h) && @ 2pm (3h)
- What: **Present** to the rest of the class the project
Contacts and Office Hours

Marco D. Santambrogio
- Contact:
  - email: marco.santambrogio@polimi.it
  - skype: marco.santambrogio
  - office: 3492 (DEI, first floor)