Overview

- Godson-3 is the third generation of the Godson microprocessor series developed by ICT at the Chinese Academy of Sciences.
- Main features:
  - Scalable architecture.
  - Reconfigurable CPU core and L2.
  - RISC processor with x86 binary translation speedup.
  - Clock speed: 1.0 GHz on a 65nm process design.
  - Low power consumption (10 w).
- Godson chips are manufactured by ST-Microelectronics and are available under the brand name Loongson.
CPU core description

- The technical name of the Godson-3’s core is GS464.
- Nine stages dynamical pipeline
  - The instruction pipeline allows to fetch 4 instruction per cycle.
  - The decoded instructions are issued to five fully pipelined function unit.
- GS464 uses out-of-order execution to improve pipeline efficiency. Its scheme combines:
  - Register renaming.
  - Dynamic scheduling.
  - Branch predicition.

CPU core description

- 64-entry register file for fixed-point and floating-point register mapping.
- 16-entry reservation station for fixed-point and 16-entry RS for floating-point (64-entry reorder queue).
- 2 fixed-point functional units (ALU1 and ALU2).
- 2 floating-point functional units (FALU1 and FALU2).
- L1 cache (four-way set associative):
  - 64 KB instruction cache.
  - 64 KB data cache.
- L2 cache (four-way set associative): 512 KB.
CPU core description

Scalable Interconnection Network

- Godson-3’s interconnection network is scalable because the same scheme can be used for implementation with 4, 8 or 16 cores.
- Godson-3 uses a mesh: each node in the mesh includes a 8x8 crossbar.
- The 4-core, 8-core and 16-core Godson-3 chips take 1, 2 and 4 node in the mesh respectively.
Scalable Interconnection Network

- The crossbar connects 4 processor as 4 masters, 4 shared L2-cache banks as 4 slaves. The remaining eight are available for connecting to other nodes.
- A second-level crossbar inside the node connects the DDR2/DDR3 memory controllers to L2-cache banks.
- The Godson-3 I/O controller is connected to the free crossbar ports of boundary nodes.
- The Godson-3 interconnection network takes the 128 bit AXI standard interface, which is simple, efficient and open.

Reconfigurable architecture

Godson-3’s reconfigurability involves 3 features:

1. Reconfigurability of the processor cores: depending on the application, the Godson-3’s AXI ports can be configured to contain either general-purpose GS464 cores or special purpose cores (Gstera).
2. The possibility to have dynamic L2 cache blocks migration to improve the locality of memory accesses. Each channel in the AXI crossbar has reconfigurable address windows, which let the software dynamically bind memory addresses to cache block locations.
3. Reconfigurability of DMA engine: software can decide if the DMA data is to or from main memory, or to or from the L2 cache directly.
X86 to MIPS translation

- Godson-3 provides hardware support for binary translation from x86 to MIPS.
- ICT engineers have added 200 instruction in MIPS format for function that are in x86 ISA but not in MIPS 64 ISA.
- No commercial RISC processor provides dedicated support for x86 emulation because of the difference between x86 and MIPS.
- Software-based translation from x86 binary to MIPS binary in inefficient.
X86 to MIPS translation

Example: x86’s Eflags.
- In x86 conditional branches are based on conditional code or flags: these are particular bits of a register, called Eflag, that are set to 1 as consequence to an ALU cycle.
- Most common flags indicate if the result of the operation in zero (ZF), if it’s negative (SF), if it has determinated carry (CF) or if it has generated overflow (OF).
- GS464 provides an Eflag equivalent instruction for each fixed-point arithmetic instruction.
- This translation can be performed by adding a SetFlag to the original instruction: this new instruction generates the x86 Eflags instead of the result of the original instruction.

X86 to MIPS translation

- Performance results of the binary translation.
- 100% performance represents the execution of native MIPS code.
- Columns represents the execution of x86 with and without hardware support.
Conclusion

• Godson-3 is a significant improvement over the Godson-2: each new version of Godson has tripled the performance of its previous one.
• Godson-3 moves Chinese microprocessor technology closer to the state of the art, although it still lags behind microprocessor produced by Intel or AMD.
• Godson-3 will advance China’s quest for greater technology independence, a vital part of the nation’s long-term economic strategy.

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