Bahurupi: A Polymorphic Heterogeneous Multi-core Architecture

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Introduction:

The distinction between high-performance embedded architecture & general-purpose computing architecture is rapidly disappearing.

What do we except from a smartphone?
Features:

- A polymorphic heterogeneous multi-core architecture
- Can be tailored according to the workload by software
- Fabricated as a homogeneous multi-core system containing multiple identical, simple cores.
- Main Novelty: its ability to morph itself into a heterogeneous multi-core architecture at runtime under software directives.
Advantage:

Solving the conflicting requirements of TLP & ILP applications

And

Achieves the seamless transition between ILP & TLP.
A high-level overview of Bahurupi architecture
Bahurupi Execution Model

Bahurupi reconﬁgurable multi-core architecture allows cores to form coalition

What is a coalition?
A group of cores working together to speedup the execution of a serial stream of instructions
A core fetches & executes one basic block of instruction at a time.

The Goal is:
To execute the basic block in parallel on the cores that form coalition.
To achieve the execution model of Bahurupi

- Resolve registers AND memory dependencies
- To ensure the cores fetch, rename and commit the basic blocks in program order

The main speedup of Bahurupi comes from the out-of-order parallel execution of instructions from different basic blocks on different cores
**Sentinel instruction:**

Compiler detects live-in & live-out registers to correspond to each basic block.

Next step: to communicate the live-in & live-out information to the hardware architecture.

So introduce a new instruction called: Sentinel.

To encode this information:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-40</td>
<td>OPCODE</td>
</tr>
<tr>
<td>36-35</td>
<td>BB_SIZE</td>
</tr>
<tr>
<td>35</td>
<td>BB_TYPE</td>
</tr>
<tr>
<td>34-29</td>
<td>LI_0</td>
</tr>
<tr>
<td>28-23</td>
<td>LI_1</td>
</tr>
<tr>
<td>22-17</td>
<td>LI_2</td>
</tr>
<tr>
<td>16-11</td>
<td>LO_0</td>
</tr>
<tr>
<td>10-5</td>
<td>LO_1</td>
</tr>
<tr>
<td>4-0</td>
<td>LO_2</td>
</tr>
</tbody>
</table>

The sentinel instruction format.
Bahurupi Execution Model requires:

a) in-order fetching of the sentinel instruction
b) In-order commit of the instruction across the cores
Architectural Details:

1. live-in register renaming
2. live-out register renaming
3. Branch Misprediction & Exceptions
4. Memory Heirachy
5. Compiler Supports
Conclusion:

Bahurupi: a reconfigurable multi-core architecture

Bahurupi: can dynamically merge the base 2-way out-of-order execution engine

Bahurupi: a hardware-software cooperative solution
Thanks for your attention
Bahurupi distributed execution model

(a) Control flow graph (CFG) of a program, and (b) Execution of the CFG on 2-core Bahurupi architecture.