Architectures for Multimedia Systems

TILERA – TILE64™ PROCESSOR

Mondello Filippo
722955
Index

- Tile Processor Architecture
- Tile64 implementation
- Tile Processor Architecture innovations:
  - Large number of tiles on a chip
  - iMesh
  - Multicore coherent cache
  - Multicore Hardwall technology
  - Multicore Development Environment Tools Suite
Tile Processor Architecture

- MIMD machine
- 2D grid of 64 homogeneous, general-purpose compute elements: tiles
- Tilera’s iMesh on-chip network
- 4 DDR2 controllers + I/O controllers

TILES:
- Processor
- L1 & L2 cache
- non-blocking switch
Tile Processor Architectures
Tile64 implementation

- Cores: 32-bit, RISC, VLIW, 90nm technology
- 192 billion 32-bit ops; 256 billion 16-bit ops; half a teraops 8-bit operations

- Memory
  - L1 cache: 8KB I, 8KB D, 1 cycle latency
  - L2 cache: 64KB unified, 7 cycle latency
  - Off-chip main memory, ~70 cycle latency
  - 32-bit virtual address space per process
  - 64-bit physical address space
  - Instruction and data TLBs
  - Cache integrated 2D DMA engine
iMesh network

• Using multiple processors require a system to allow communication among them.
  ◦ Old Solution: bus interconnection.
  Problem: more cores added to chips → bus creates data congestion, limiting performance scalability with the increased number of cores
  ◦ Tilera’s solution: iMesh

• iMesh:
  • user dynamic network (UDN)
  • I/O dynamic network (IDN)
  • static network (STN)
  • memory dynamic network (MDN)
  • tile dynamic network (TDN).
iMesh network

- Each tile uses a fully connected crossbar → all-to-all five-way communication.
- Dynamic networks:
  - packetized, fire-and-forget interface, dimension-ordered wormhole-routed.
  - Packet = header word + up to 128 words per packet
  - Hop latency:
    - one cycle if packets are going straight
    - one extra cycle for route calculation when a packet must make a turn at a switch.
- Static network:
  - static configuration of the routing decisions at each switch point.
  - auxiliary processor for reconfiguring the network in a programmatic manner.
iMesh network

- UDN $\rightarrow$ userland processes or threads
- IDN $\rightarrow$ direct communication with I/O devices.
- MDN $\rightarrow$ communication with off-chip DRAM.
- TDN $\rightarrow$ direct tile-to-tile cache transfers. Works in concert with the MDN.
- STN $\rightarrow$ low-latency, high-bandwidth channelized network — great for streaming data.
Multicore coherent cache

- Cache subsystem → high-performance, two-level, non-blocking cache hierarchy.
- Each tile's cache can be shared with other tiles → each tile can access the aggregate multi-megabyte cache.
- Each tile can view the collection of on-chip caches of all tiles, serving as an L3 cache.
- Neighborhood caching to provide an on-chip distributed shared cache.
**Multicore Hardwall technology**

- Enables the user to define one or many cores as a processing island, eliminating communication between it and other cores unless specified.
- If a packet attempts to cross the established boundary, an interrupt is signaled and control is passed on to the hypervisor.
- Tile Processor architecture results well suited to hosting multiple operating systems running independent applications, or multiple instances of the same application, on a single-chip platform.
The Tilera MDE includes a powerful Eclipse-based integrated development environment (IDE), an ANSI-standard 'C' compiler, a full-system simulation model and a set of flexible command-line interfaces.

To achieve optimum performance on the chip, the MDE includes an optimized user communication library (iLib) offering standard mechanisms such as process management, socket-like streaming channels, message passing, and shared-memory communication.

Tilera defined the Tilera’s Gentle Slope Programming model which enables the user to begin with familiar programming tools and move to advanced, large-scale multicore programming easily.
References:

- http://techreport.com/discussions.x/13069
- http://www.hwupgrade.it/news/portatili/64-core-per-il-processore-tile64_22252.html
- http://www.theregister.co.uk/2007/08/20/tilera_tile64_chip/
- http://www.tgdaily.com/content/view/33451/135/
- http://www.pcmag.com/article2/0,1895,2173203,00.asp