ACA Student Assignment/Project Description

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Dipartimento di Elettronica e Informazione
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Optional Oral Presentations
Optional Oral Presentations

- MAXIMUM ADDITIONAL SCORE: 2 points

- Description:
  1. Selection of a research paper of interest from a given list
  2. Study of the selected paper and the referenced material
  3. Presentation of the paper in the classroom in front of the rest of students

- Rules:
  1. STRICT DEADLINE: 18 JUNE 2012. All presentations will take place during the scheduled lesson hours.
  2. PRESENTATION (SINGLE PERSON): MIN 10 MAX 12 SLIDES IN ENGLISH
  3. PRESENTATION (TWO PERSONS): MIN 15 MAX 20 IN ENGLISH
  4. First-Come-First-Serve procedure will be followed
List of proposed papers (1-7)

1. SPARC T4: A Dynamically Threaded Server-on-a-Chip
2. Task Superscalar: An Out-of-Order Task Pipeline
3. The IBM BLUE GENE/Q Compute Chip
4. Bahurupi: A Polymorphic Heterogeneous Multi-Core Architecture
5. AMD Fusion APU: LLANO
6. GODSON-T: An Efficient Many-Core Processor Exploring Thread-Level Parallelism
7. The SARC Architecture
Many-Core Accelerator Architectures

1. COOL MEGA-ARRAYS: Ultra Low-Power Reconfigurable Accelerator Chips
2. REMAP: A Reconfigurable Architecture for Chip Multiprocessors
3. RIGEL: A 1024-Core Single-Chip Accelerator Architecture
4. The accelerator store - A shared memory framework for accelerator-based systems
5. Making wide-issue VLIW processors viable on FPGAs
List of proposed papers (13 - 18)

- Power and Variability Aware Processor Design
  1. Power Management Architecture of the Intel Architecture Code-Name Sandy Bridge
  2. Resilient Architectures via Collaborative Design: Maximizing Commodity Processor Performance in the Presence of Variations
  3. Temperature-Aware Scheduling and Assignment for Hard Real-Time Applications on MPSoCs
  4. Voltage Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software-Guided Thread Scheduling
  5. Power Gating Strategies on GPUs
List of proposed papers (19 - 25)

- Memory Architecture Design
  1. Hardware Transactional Memory for GPU Architectures
  2. Hardware/software techniques for DRAM thermal management

- Interesting Modern Research Ideas/Analysis in CompArch
  1. Design Space Exploration for 3D Architectures
  2. Implementing domain-specific languages for heterogeneous parallel computing
  3. A Predictive Model for Dynamic Micro-architectural Adaptivity Control
  4. Indoor localization without infrastructure using the acoustic background spectrum
  5. Scaling with Design Constraints Predicting the Future OF Big Chips
Optional Project Assignments
Optional Project Assignments

- MAXIMUM ADDITIONAL SCORE: 5 points

- Description:
  1. Selection of project from a given list
  2. Preparation of the project assignment
  3. Deliver of the project material + short description for evaluation

- Rules:
  1. DEADLINE: FIRST BATCH: 11 JULY 2012
     SECOND BATCH: 11 SEPT 2012
  2. For request a project assignment send an e-mail to xydis@elet.polimi.it with the title: [ACA COURSE: PROJECT ASSIGNMENT - TITLE OF PROJECT]

     Assignments will be made in a FCFS manner.
Type 1: Study of the impact of micro-architectural and/or design parameters

1. For a given simulator record its input parameters and its output metrics.

2. Experiment with the simulator

3. Link the simulator with the Multicube DSE framework through writing the XML files

4. Perform small exploration with GIVEN script

**Technical requirement:** Simple scripting to read file of parameters/metrics and write the XML file
1. For the given simulators record its input parameters and its output metrics.
2. Experiment with the simulators
3. Link the output of simulator A to the input of simulator B
4. Perform combined simulations

- **Technical requirement**: Simple scripting to read file of metrics from sim_A and write the input file of sim_B
Type 3: Internal modification/extension of simulator

1. Install and experiment with the simulator and/or design tool
2. Extend the fields of the data structures to capture new information if needed
3. Add simple or given already functions in order to model the metrics
4. Perform simulation reporting the new outputs

- **Technical requirement**: Coding in C/C++ for the modifications and/or simple scripting for dumping/reporting results
Type 4: Code development for solving real but “simple” architectural design problems

1. Understand of the design problem and the given algorithmic solution
2. Code for parsing the given problem inputs
3. Code for engineering the proposed algorithm for the problem solution
4. Experiment with the developed program

- **Technical requirement**: General coding i.e. C/C++, bash script, perl etc
Proposed project topics (1-8)

- Multi-/Many-Core architectures:

1. Design space exploration of GPGPU.s. *(Type 1)*
2. Design space exploration of NoC multicore with GEMS. *(Type 1)*
3. Thermal aware simulation of CMP multi-core architectures. *(Type 2)*
4. Power/Temperature Analysis of heterogeneous many-core. *(Type 2)*
5. Runtime temperature monitoring of simulated multi-core. *(Type 2)*
6. Implementation DVFS in simulated multi-core architectures. *(Type 3)*
7. Analysis of voltage emergencies (IR drop) in simulated single or multi-core architectures. *(Type 3)*
8. Post-scheduling thermal-aware optimization of VLIW architectures. *(Type 4)*
Proposed project topics (9-16)

- Custom Processor/Accelerator Synthesis:

  1. Coarse-grained reconfigurable processor design with NISC. *(Type 1)*
  2. Cross-application predictability for customized coprocessor synthesis. *(Type 1)*
  3. Integration of customized HLS generated coprocessor integration in FPGA-based multi-processor. *(Type 2)*
  4. Reconfigurable-VLIW synthesis on FPGA. *(Type 2)*
  5. Experimenting with the Fabscalar framework for RTL synthesis of single and multi-core architectures. *(Type 2)*
  6. Scripting based HLS: XML modularization of Legup/Bambu HLS scheduling/binding/Verilog generation. *(Type 3)*
  7. Thermal-aware timing-slack scheduling for High Level Synthesis generated processors. *(Type 4)*
  8. Thermal aware operation binding during coprocessor synthesis. *(Type 4)*
Emerging 3D processor/memory technologies:

1. Temperature simulation/analysis of emerging 3D-IC multi-core systems. *(Type 1)*
2. Thermal issues in 3D-CMP multi-cores. *(Type 2)*
3. *Micro-architecture simulator with a 3D cache memory hierarchy.* *(Type 2)*
4. *Micro-architecture simulator with a 3D DRAM.* *(Type 2)*
5. Memory organization analysis by integrating DRAMSim to to analyze the impact of Last Level Cache parameters. *(Type 2)*
Proposed project topics (22-25)

- Run-time management for multi-core:
  1. Integrating and monitoring MIND based version of SVC video application with BOSP RTRM system. (Type 4)
  2. Implementation of a simple CPU-manager for shared-memory many-core architecture. (Type 4)

- New Design Space Exploration tools:
  1. Internet in the loop Design Space Exploration (Type 4)
  2. Web interface for Simplified Design Space Exploration. (Type 4)
Discussion Questions/Clarification