CV SUMMARY - CRISTINA SILVANO

I am currently **Associate Professor (with tenure)** of Computer Engineering at Politecnico di Milano (DEIB). In December 2013, I have received the Scientific National Qualification in Italy as **Full Professor** in sector 09/H1 Information Processing Systems and in sector 01/B1 Informatics (as defined in DD222 of July 20, 2012).

RESEARCH ACTIVITIES

My current research focuses on Computer Architecture and Electronic Design Automation, with emphasis on power-aware design, design space exploration of embedded architectures, adaptive design and monitoring of applications for many-core architectures, many-core architectures based on Networks-on-Chip, technology-aware many-core architectures. **Highlights of my recent research can be found in the following 5 research papers: ACM Trans. on Embedded Computing Systems 2013** [J4], **ACM Trans. on Embedded Computing Systems 2012** [J7], **IEEE Trans. on CAD 2009** [J10], **IEEE Trans. on Computers 2008** [J11], **IEEE Trans. on VLSI Systems 2006** [J15].

RESEARCH PROJECTS AND INTERNATIONAL COLLABORATIONS

My research activities have been carried out in collaboration with several international universities, research centers and industries (about **90** out of my **140** scientific publications include co-authors with different affiliations, **35** out of them with industrial co-authors, **106** co-authors overall). My research has been funded by several national and EU projects selected based on a competitive process. Since 2003 I was co-applicant and active participant of **7** European and **2** industrially funded projects (attracting around **3.5 M€** funding for POLIMI). Among them, I was **Project Coordinator of two European projects: FP7-2PARMA (2010-2013)** and previously **FP7-MULTICUBE (2008-2010).** Since 1996 I have started a continuous research collaboration with **STMicroelectronics** on power-aware embedded architectures. I was **Principal Investigator** of **2** industrial research projects funded by STMicroelectronics (2003-2008).

SCIENTIFIC OUTCOMES

My scientific production consists of more than **140** publications:

- Co-author of **27** top-ranked journal publications including **16 IEEE/ACM Transactions: 6** IEEE Trans. on CAD, **5** IEEE Trans. on VLSI Systems, **3** ACM Trans. on Embedded Computing Systems, **1** IEEE Trans. on Computers, **1** IEEE Trans. on Information Theory; Co-author of **13** chapters in scientific books;
- Co-author of more than **90** scientific publications on peer-reviewed conferences/workshops including **33 top-level conferences** (**17** DATE, **8** CODES-ISSS, **3** ASP-DAC, **2** DAC, **2** CASES and **1** ICCAD) collecting one Best Paper Award, one HiPEAC paper award and one of the most influential papers published at DATE conference in the decade 1998-2008;
- Co-author of the scientific book: "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", Kluwer Academic Publisher (2003);
- Co-author of the academic textbook (in Italian): "Progettazione Digitale" (Logic Design), McGraw-Hill (2002, 2007);
- Co-editor of **2** scientific books: "Low-Power Networks-on-Chip", Springer (2010) and "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011);
- Inventor/Co-inventor of **11 patent applications** with Group Bull or STM **(7 out of 11 already granted)**.

Based on Google Scholar (03/12/2014), my h-index is **25**, my i10-index is **58** and my total number of citations is **2270**.

SCIENTIFIC SERVICES

I am an active contributor to the scientific community and I regularly serve as **Member** (or **Track Chair**) of the Program Committee of several top-level conferences such as **ICCAD, DAC, DATE, NOCS, HPCA, MICRO, ASAP, FPL**. I was **Program Co-Chair** of **ASAP2012, ARC2011,** and **SASP2010.** I was **General Co-Chair** of **SASP2009** and **MICRO2008** (receiving the ACM Recognition of Service Award). I have also organized several international workshops as **Program** or **General Chair**. I was **Guest Co-Editor** of **two** special issues on journals and **Associate Editor** of MICPRO Journal (Elsevier). I am **Senior Member of IEEE** (since 2009). I have served as **Independent Expert Reviewer** for the European Commission and for several science foundations such as the **Agence National de la Recherche** (F), **INRIA** (F) and the **Academy of Finland.** I have been invited to give several Invited Talks / Seminars/ Panels all over the world.

ACADEMIC SERVICES

I have balanced my effort in teaching at Undergraduate and M.Sc. level. I annually teach basic courses on Computer Architectures and Operating Systems and M.Sc. courses on Advanced Computer Architectures. I enjoy teaching and I have an extensive English-speaking teaching experience at Como Campus of POLIMI and at USI (CH). I am an active contributor to the organisation of teaching activities and tracks in Computer Engineering at POLIMI, mainly at Como Campus. I am Chair of the Committee on Undergraduate Study Plans, Chair of the Committee on Undergraduate Transfers and Member of the Committee on Undergraduate Studies and Member of the Committee on Graduate Admissions and. I was advisor of **60+ M.Sc. students** and advisor/co-advisor of **11 Ph.D. students**. Currently, I am advisor of **3 Ph.D. students** and my **research staff** is composed of **two** faculty members and **two** post-doctoral researchers.

INDUSTRIAL EXPERIENCE

I have started my career as **Design Engineer** and then **Senior Design Engineer** at the **R&D Labs of Group Bull** in Italy (1987-1996). Since 1992, I was part of the **Bull-IBM Research** team for the design of the first worldwide multiprocessor system based on **PowerPC** architecture. These multiprocessors have been commercialized as **Bull Escala** UNIX Servers and as **IBM RS/6000** Multiprocessor Servers. I have also spent several periods abroad as **Visiting Engineer** at Bull R&D Labs, Billerica (MA - USA), **Visiting Engineer** at VLSI Technology, in Munich (D) and in S. Jose (CA-USA) and **Visiting Engineer** at IBM Somerset Design Center, Austin (TX - USA).

CURRICULUM VITAE - CRISTINA SILVANO

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1. PERSONAL DATA AND CAREER

CRISTINA SILVANO, PH.D.
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Born in Milan (Italy), December the 25th, 1961. Living in Milan (Italy).
Languages: Italian (mother tongue); English (fluent); French (good reading and listening); Spanish (basics).

My career is twofold. In 1987, after graduation at Politecnico di Milano, I have started my ***industrial career*** as Design Engineer (then upgraded as Senior Design Engineer) at the R&D Labs of Group Bull (Italy) spending several periods abroad as Visiting Engineer. Almost a decade later, to follow my interests in the scientific research and my attitude towards teaching, I have started my ***academic career*** as Ph.D. student at Università degli Studi di Brescia (Italy). After my Ph. D., received in 1999, I have continued as Post-Doc Researcher at CEFRIEL and at Politecnico di Milano, Assistant Professor at Università degli Studi di Milano (2000-2002) and Associate Professor at Politecnico di Milano (2002-present).

1.1. EDUCATION

- **Dottorato di Ricerca in Ingegneria dell'Informazione (Ph.D. in Computer Engineering)**, Università degli Studi di Brescia (Italy), 1999. Ph.D. Thesis on: "Power Estimation and Optimization Methodologies for Digital Circuits and Systems", Advisor: Prof. P. Gubian, Università degli Studi di Brescia, Co-Advisor: Prof. D. Sciuto, Politecnico di Milano.
- **Laurea in Ingegneria Elettronica (Master of Science in Electrical Engineering),** Politecnico di Milano, 1987 (Final grade 100/100). MS Thesis on: "Theoretical and numerical study of shallow waters fluid dynamic models", Advisor: Prof. G. Prouse, Politecnico di Milano, Co-Advisor: Prof. L. Gotusso, Politecnico di Milano.

1.2. ACADEMIC CAREER

- In December 2013, I have received the Scientific National Qualification in Italy as **Full Professor** in sector 09/H1 Information Processing Systems and in sector 01/B1 Informatics (as defined in DD222 of July 20, 2012).
- **Associate Professor** (from 01/09/2002; **with tenure** from 01/09/2005) in Computer Engineering at Politecnico di Milano, Department of Electronics, Computer Engineering and Bioengineering (DEIB). I annually teach basic and advanced courses on Computer Architectures and Operating Systems. My primary research interests are in the areas of Computer Architecture and Electronic Design Automation, with particular emphasis on power-aware design, design space exploration for embedded architectures, adaptive design and monitoring of applications for many-core architectures, many-core architectures based on Networks-on-Chip, technology-aware many-core architectures and fault tolerant coding techniques.
- **Assistant Professor** (01/10/2000 - 31/08/2002) in Computer Science at Università degli Studi di Milano, Department of Computer Science. I was annually teaching basic and advanced courses on Computer Architectures and Operating Systems. My research activity was mainly focused on power-aware computing for embedder processor architectures.
- **Post-Doc Researcher** (Assegnista di Ricerca) (01/9/1999 - 30/09/2000) at Politecnico di Milano, Dipartimento di Elettronica e Informazione. Main research topic: "Computing Architectures: testing and simulation systems" (Supervisor Prof. D. Sciuto, Politecnico di Milano). My research activities were also related to the research project on *"Power estimation methodologies for VLIW architectures",* in collaboration with STMicroelectronics.
- **Post-Doc Researcher** (01/01/1999 - 31/08/1999) at CEFRIEL (Center for the Research and the Education in Information Engineering, Milan), Electronic Design Automation Area. My research activity was mainly part of the research project TOSCA (Tools for System Co-design Automation) and the European Project No. 26796 PEOPLE (Power Estimation for fast exPLoration of Embedded systems) under the supervision of Prof. D. Sciuto.
- **Ph.D. Student** (01/03/1996 – 31/12/1998) at Università degli Studi di Brescia (Italy), Dipartimento di Elettronica per l'Automazione. My research activity was mainly focused on power estimation and optimization methodologies for embedded architctures. Ph.D. defense held in 1999.

1.3. INDUSTRIAL CAREER

From May 1987 to February 1996, I was employee at the **R&D Laboratories of Groupe Bull** (also known as Bull HN Information Systems), Pregnana Milanese (Italy) where I held the position of **Design Engineer** up to March 1993 and **Senior Design Engineer** up to February 1996. During my experience at Groupe Bull, I have been involved in the following research and development activities:

- From September 1988 to October 1990, I was part of the design team of a full-custom 32-bit Central Processing Unit including a virtual memory management unit. The CPU was designed for a system based on the GCOS6 Bull proprietary OS. During the design, I was **Visiting Engineer** at the **Bull R&D Labs, Billerica (MA - USA)** in Fall 1988 and in Spring 1989. I also was **Visiting Engineer** at the VLSI design center of **VLSI Technology Inc., Munich (Germany)** from February-March 1990, and at **VLSI Technology Inc. in S. Jose (CA-USA)** in April 1990. For my contribution to the microprocessor design and verification, I received the **"1991 Bull Technical Award"**.
- In 1990, I designed a Dual Port SRAM module generator based on a process-independent design methodology. The generator has been used to synthesize two embedded memories integrated in a VLSI circuit designed for the European project ESPRIT2 -IDPS (Integrated Design and Production System) No. 5075 (1990-1992). In 1992, I have applied as co-inventor of a hierarchical and modular memory architecture in one **European patent** [P1-EU] granted in 1997.
- From 1991 to July 1992, I was with the Bull Advanced Technology Group, responsible for the introduction of new technologies and methodologies in the design of integrated circuits for Bull computer systems.
- Since August 1992, I was part of the **Bull-IBM Research (Austin-US)** design team of the chip set for the Bull Escala multiprocessors, which are symmetric and scalable systems based on shared memory architecture and composed of two to eight processors. The Escala systems have been **the first worldwide multiprocessors based on the PowerPC architecture** (introduced in 1992 by the Apple-IBM-Motorola alliance, then generating the PowerPC 601, 604e e 620 processors). The first implementation of the architecture was the PowerPC 601 released by IBM in 1992. The Escala systems have been fully developed at the R&D Bull Labs in Italy by a Bull-IBM joint team and then commercialized as **Bull Escala UNIX Servers** and **IBM RS/6000** Symmetric Multiprocessor Servers (named also as **RS/6000 POWERserver** servers, **RS/6000 POWERstation** and then renamed as **eServer pSeries** in October 2000). During the Bull-IBM joint project, I also was **Visiting Engineer** at **IBM Somerset Design Center, Austin (TX - USA)** in Fall 1993 and in Spring 1994. For the research and development of the Escala/RS6000 multiprocessor systems, my main contributions were:
  - From August 1992 to May 1993**,** I was in the design team of the chip-set implementing the 64-bit data cross bar architecture, named **PowerScale,** connecting four processor nodes (including two processors each), the I/O node (including two I/O channels), and the shared memory. The PowerScale architecture has been adopted by many commercial series of the Bull Escala servers. The chip-set includes a new error detection and correction code to improve system reliability and data integrity. From this code, I developed the construction techniques for a new class of codes for computer memory sub-systems. For the new class of codes, I applied as Inventor in one **European Patent (granted in 1998)** [P2-EU] and in one **US Patent (granted in 1996)** [P2-US].
  - From June 1993 to July 1994, I was in the design team of a 120K gates VLSI circuit with the functionality of Secondary Cache Controller for both PowerPC 601 and 604 processors. The circuit implements the cache coherency mechanism both vertically (between the different cache levels of each processor) and horizontally (among different processors). The cache coherency is based on the MESI protocol.
  - From September 1994 to December 1995, I was in the team for the design and simulation of a 230K gates VLSI circuit with the functionality of Memory Controller**,** based on a shared and interleaved memory sub-system. The circuit manages also the data-cross bar architecture, PowerScale, for the new series of multiprocessor systems: Escala-E and Escala-T. More in detail, The Escala-E servers support up to two processors (PowerPC 604e or 620), the shared memory configurable from 16MB to 2 GB, and a single 64-bit PCI bus. The Escala-T servers support up to four processors (PowerPC 604e or 620), the shared memory configurable from 32 MB to 3 GB, and two 64-bit PCI buses.
- During the Academic Years 1993/94 and 1994/95, I also held the position of **Bull Senior Researcher,** supervisor of some Master students in Information Technology at **CEFRIEL** – Research and Training Center in Milano in the Electronic Design Automation area. The activities were partially funded by the European Project EUREKA/JESSI (Joint European Submicron Initiative) – Subprogram Application AC-5.

2. RESEARCH ACTIVITIES

2.1. RESEARCH TOPICS AND MAIN ACHIEVEMENTS

My research is primarily focused on the areas of **Computer Architectures** and **Electronic Design Automation,** with particular emphasis on the following research topics *(listed hereafter in chronological order).* For each research topic, the most significant achievements are also reported.

2.1.1. Fault Detection and Fault Tolerant Coding Techniques

The research faced with Error Control Coding techniques to improve the fault detection and fault tolerance in computing systems. Main goals of the research were, from one side, the design of a new class of error detection and correction codes and, from the other side, the definition of detection codes for unidirectional errors. Starting from the proposed coding schemes, a set of automatic tools to support the design of the proposed coding techniques has been defined.

Main achievements: My contribution to the field was the introduction of a new class of systematic SEC-DED (Single Error Correction – Double Error Detection) codes with single byte error detection capability published in **IEEE Trans. on Information Theory 1995** [J27]. An automatic code generation framework was developed and published in **IEEE Trans. on VLSI 1998** [J24]. For the new class of codes, I have been designated as **inventor** in both the **European Patents** [P2-EU] granted in 1998 and in the **US Patent** [P2-US] granted in 1996. An implementation of the new class of error detection and correction codes has been part of the PowerScale architecture commercially adopted by the **Bull Escala** and **IBM RS6000** multiprocessor systems.

2.1.2. Power-Aware Computing for Embedded Architectures

Power dissipation has been identified as the main performance limiter for high-performance processors, while power dissipation limits the capabilities of battery-powered embedded mobile devices and wireless sensor nodes. My research on power-aware design started in 1996, at the beginning of my Ph.D. program (under the supervision of my co-advisors, prof. P. Gubian and prof. D. Sciuto). The main goal of my Ph. D. research was to develop design techniques for the analysis and synthesis of digital circuits and systems to reduce the power consumption at the higher levels of abstraction. The research activity was mainly focused on the estimation and optimization of power dissipation. Then I started my Post-Doc at Politecnico di Milano (under the supervision of my mentors, prof. D. Sciuto and prof. M. Sami) and my research moved towards the investigation of power-aware techniques for embedded architectures based on VLIW (Very Long Instruction Word) pipelined processors. My post-doc research on low-power VLIW architecture has been carried out in collaboration with Vittorio Zaccaria (at that time Ph.D. student at Politecnico di Milano). The proposed techniques have been applied to the **Lx/ST200** family of VLIW embedded processor cores (developed as a partnership between HP Labs and STMicroelectronics). The ST200 family (including the ST210, ST220, ST231 processor cores) is still used today for embedded media processing in a variety of audio, video and imaging consumer products.

Main achievements: The most significant achievements of my Ph.D. thesis on high-level power estimation have been published in **IEEE Trans. on VLSI-1998** [J25] and **JSA-1997** [J26]. My Ph.D. thesis research represents one of the first efforts to face the problem of power-aware bus encoding for processor-to-memory communication by exploiting spatial-temporal locality. Main achievements of my Ph.D. thesis related to low-power bus encoding techniques have been published in **GLS-VLSI-1997** [C84] and **DATE-1998** [C81]. These two early papers in my career have had a high research impact (so far, they have had **281** and **136** citations respectively, still representing my top ranked papers). The paper presented at **DATE-1998** [C81] has also been selected in 2008 as a chapter of the volume: *"The Most Influential Papers of 10 Years DATE"* [CH11]. For the design of a low-power encoder/decoder architecture (developed in collaboration with STMicroelectronics), I have been designated as co-inventor in the **European Patent Application** [P3-EU] published in 2001 and in the **US Patent Application** [P3-US] published in 2002.

The most significant achievements of my Post-Doc research were: *(i)* to develop the first and most comprehensive power estimation framework at the instruction-level validated on an industrial VLIW architecture (the Lx/ST200 family), *(ii)* the definition of an innovative register file write inhibition scheme to exploit forwarding paths is the pipeline to save power when accessing short-lived variables; *(iii)* the definition of power-aware branch prediction techniques based on compiler hints for VLIW processors. More in detail, the instruction-level energy model for VLIW pipelined processors has been published in **CODES-2000** [C72], **ICCAD-2000** [C70] and then extended to the **IEEE Trans. on CAD-2002** [J22]. Results on the reduction of the complexity of the energy model by introducing the concept of instruction clustering have been presented in **DAC-2002** [C64], then extended in **DAES-2005** [J18] and **PATMOS-2001** [C66]. Results on power optimization of the pipeline forwarding paths and branch prediction for VLIW have been published in **DATE-2001** [C69], **GLS-VLSI-2003** [C60], **GLS-VLSI-2004** [C57] then extended to **IEEE Trans. on VLSI-2002** [J20] and **Integration-2005** [J19]. For the low-power forwarding architecture, I have been designed as co-inventor in the **US Patent** [P4-US] **granted in 2005.** Finally, most significant contributions on power-aware VLIW design techniques have been collected in 2003 in the **scientific book**: *"Power Estimation and*

Optimization Methodologies for VLIW-based Embedded Systems" [B1] published by Kluwer Academic Publishers.

The research experience and accomplishments on power-aware computing lead me towards one of my primary **on-going** research paths: design space exploration techniques for computing architectures from a combined power/ performance perspective.

2.1.3. Design Space Exploration of Embedded Architectures

Given the complexity of multi/many core architectures, system optimization and exploration definitely represent challenging research tasks. A wide range of design parameters must be tuned from a multi-objective perspective, mainly in terms of performance and energy consumption, to find the most suitable system configuration for the target application. Multi-objective exploration of the huge design space of multi/many core architectures definitely needs for automatic **Design Space Exploration (DSE)** techniques to systematically explore the design choices and to compare them in terms of multiple competing objectives (trade-offs analysis). The aim of my research (carried out mainly in collaboration with Vittorio Zaccaria and Gianluca Palermo) was to investigate on power/performance trade-offs in application-specific embedded architectures. The exploration techniques are based on multi-objective optimization algorithms and energy/delay estimation metrics. The main goal is to provide an automatic DSE methodology and tool for the analysis of system characteristics and the selection of the most appropriate architectural solution to satisfy power/performance system requirements. A set of heuristic optimization algorithms have been defined to prune the design space to be explored, while a set of response surface modeling techniques have been defined to further speed up the exploration time. The basic idea was defining an analytical response model of the system behavior based on a subset of system simulations to predict the unknown system response. The proposed DSE framework (namely MULTICUBE Explorer) leverages a set of open-source tools for the exploration, modeling and simulation to guarantee a wide exploitation of the project results in the embedded system design community. Research on DSE techniques have mainly been carried out in the context of the **FP7-MULTICUBE** European project under my scientific coordination.

Main achievements: The primary contribution of my research was to define an automatic multi-objective DSE methodology and related framework (MULTICUBE Explorer) to tune embedded on-chip platforms finding the best power/performance trade-offs, while meeting system-level constraints and speeding up the exploration process. Under the premises of the MULTICUBE project, MULTICUBE Explorer open-source tool has been developed and validated on STMicroelectronics and IMEC virtual platforms. Benefits of the MULTICUBE design methodology and tools have been assessed on a number of industrial use cases provided by STMicroelectronics and IMEC. The most significant results of my research on DSE have been published in top-ranked journals like **DAES-2002** [J23], **DAES-2007** [J14], **IEEE Trans. on CAD 2009** [J10], **IEEE Trans. on CAD 2012** [J8], and in several conferences, among them **CODES-2001** [C68], **DATE-2003** [C63], **SAC-2003** [C62], **GLS-VLSI-2003** [C61], **PATMOS-2003** [C59], **SAC-2004** [C58], **SASP-2008** [C43], **SAMOS-2008** [C42], **SAMOS-2009** [C33], **SASP-2009** [C32], **DAC-2010** [C26] and **SASP-2011** [C22]. More recently, main research outcomes of my on-going DSE research appeared in high-impact venues like **CODES-ISSS-2012** [C15], **DATE-2013** [C13], **DATE-2013** [C12] and **DATE-2014** [C7]. Finally, I was also **Co-editor** of the scientific book: "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Springer, 2011 [E4].

2.1.4. Adaptive Design and Monitoring of Applications for Many-core Architectures

Based on the knowledge on *design-time* multi-objective exploration, my research path evolved towards the definition of a *run-time* methodology to optimize the allocation and scheduling of different application tasks on the underlying resources of the target many-core architecture. In 2007, to address this problem, a two-step approach has been devised in collaboration with IMEC researchers and Giovanni Mariani (Ph.D. student at University of Lugano, CH). First, the design exploration flow generates a Pareto-optimal set of design alternatives in terms of power/performance trade-offs. Second, this set of operating points can be used at *run-time* to decide how system resources should be allocated to different tasks running on the many-core system. Research on run-time resource management techniques have mainly been carried out in the context of the **FP7-2PARMA** European project under my scientific coordination. During 2PARMA project, the proposed run-time methodology has been applied to several application domains to demonstrate their applicability and benefits in industrial contexts, such as the P2012/STHORM many-core platform provided by STMicroelectronics.

I believe dynamic runtime systems still provide many opportunities for energy savings. Some new research paths have recently been opened. Research is **on-going** on approximate and adaptive computing for power-aware embedded systems. Since optimizing computing systems for all worst case scenarios is not a feasible approach, we have to start thinking at systems that are capable to **self-adapt** dynamically to changing operating conditions and environments. The lack of self-tuning and run-time adaptation capabilities at the application-level tends to led to sub-optimal power/performance trade-offs at the system level given by the underutilisation of the resources in a many-core architecture. The proposed approach borrows some concepts derived from the approximate and adaptive computing area to give to the application some **self-tuning** capabilities. The system-wide adaptive approach is based on global monitoring, adaptation and optimization. Appropriate self-adaptive techniques are

provided to dynamically support migration of code and data among cores. In the context of **heterogeneous** many-core architectures, we can devise support for code and data migration between different types of processing cores, thus capable to adapt to several processor architectures and hardware accelerators. **On-going** joint research with the **Technical University of Delft (NL)** is focused on run-time optimization techniques of dynamically reconfigurable systems. I believe there are still significant paths dealing with heterogeneity in the era of many-cores based on accelerator-centric architectures.

Main achievements: The main contribution of my research was on the exploitation of the synergy of *design-time* and *run-time* techniques to get an effective approach towards a power-aware adaptive computing. The main outcomes of the research on adaptive management techniques applied to multi-core and reconfigurable architectures have been published in **DATE-2010** [C27], **IET-2011** [J9], **DATE-2012** [C17] and more recently in **FPL-2013** [C11], **ASP-DAC-2014** [C8], **PARCO-2013** [J5] and **ACM Trans. on Embedded Computing Systems 2013** [J4].

2.1.5. Many-core Architectures based on Networks-on-Chip

Given the increasing complexity of many-core architectures, the current trends on on-chip communication are converging towards the Network-on-Chip (NoC) approach, representing a high bandwidth and low energy solution. Using the NoC-based design approach has several other advantages, such as scalability, reliability, IP reusability and separation of IP design from on-chip communication design and interfacing. NoC design represents a new paradigm to design multi/many-cores shifting the design methodologies from computation-based to communication-based. To address these NoC research challenges, a new path of my research started in 2003 focusing on the topic of low-power NoC for embedded architectures, covering energy aware design and techniques from several perspectives and abstraction levels. My research on NoC started as advisor of Gianluca Palermo (at that time Ph.D. student at Politecnico di Milano) focusing on the development of **PIRATE,** a modular and flexible framework for power/performance exploration of Network-on-Chip architectures. The PIRATE framework has then been applied to explore distributed shared memory architectures based on NoC. For this class of systems, I have also started a new research path to investigate the problem of synchronization mechanisms and memory management techniques. Most of my research on low-power NoC for embedded architectures have been carried out in the context of two industrial research projects funded by **STMicroelectronics.** I was **Principal investigator** in both research contracts, namely: *"Low Power Network on Chip and Embedded Architectures"(2003-2005)* and *"Low Power Network on Chip and Multiprocessor Platforms" (2006-2008)*.

Then my research was addressing the problem of the application mapping, optimization and topology customization for the **Spidergon NoC** architecture provided by STMicroelectronics (Grenoble, F). My research on **ST Spidergon NoC** has been carried out in the context of the **MEDEA+ LoMoSA+** project.

In that period, I have started working with prof. D. Sciuto co-advising the Ph.D. thesis of Giovanni Beltrame on modeling, simulation, analysis and optimization of Multi-Processor System-on-Chip platforms. My contribution was mainly to support the Network-on-Chip modeling and exploration. The target platform has been configured to simulate an IPv4 forwarder (based on the StepNP framework developed at STMicroelectronics Research Labs, Ottawa), an MPEG4 VGA encoder, and an Ogg-Vorbis encoder. These applications have been modeled by introducing a multi-accuracy transaction-level approach, then explored and optimized in terms of power and performance.

In 2007, I have started investigating about security aspects in NoCs together with Gianluca Palermo and Leandro Fiorin (Ph.D. student at University of Lugano, CH). Our work appeared at **CODES-ISSS 2007** [C46] still remains to this day one of the first approaches to investigate an important but unaddressed aspects of NoCs, namely *security.* The work has then been extended in **IEEE Trans. on Computers 2008** [J11]. Afterwards, we opened a new research path by adding high level services on top of the standard communication services usually provided by an interconnection network. Research on **run-time monitoring** through NoC are still on-going under my scientific coordination in collaboration with **ALaRI Research Institute** based at the University of Lugano (CH). Moreover, on-going joint research with the **Universidade Federal do Rio Grande do Sul** in Porto Alegre (Brasil) is focused on floor planning-aware exploration for application-specific NoC and adaptive buffers for virtual channel routers in NoCs.

Main achievements: Main research achievement of my early research on NoC were: *(i)* the development of **PIRATE** framework for NoC optimization (presented in **PATMOS-2004** [C56]) and *(ii)* the development of **GRAPES** modeling and simulation framework for multi-processor Systems-on-Chip based on NoC presented at **IC-SAMOS-2006** [C52] and then extended in **JSA-2007** [J13]. One of the most significant results of the research team I was leading at that time at Politecnico di Milano (and composed of M. Monchiero, G. Palermo and O. Villa) was the definition of optimized ***synchronization techniques*** for distributed shared memory multi-core architectures based on Network-on-Chip. The proposed synchronization techniques appeared in high-impact venues: **DATE-2006** [C53], **ACM SIGARCH-2006** [J16], **IEEE Transactions on VLSI 2006** [J15] and then **CASES-2008** [C38].

The main outcomes of the research done in collaboration with prof. D. Sciuto and G. Beltrame have been

published in the Proceedings of top-level conferences (**CASES-2004** [C55], **DATE-2006** [C54] and **CODES-ISSS-06** [C50]) then extended in the **IEEE Trans. on CAD 2007** [J12].

Concerning our pioneer work on NoC security, the most relevant research result is represented by a data protection unit for NoC architectures presented first at **CODES-ISSS-2007** [C46] and then extended in the prestigious **IEEE Trans. on Computers 2008** [J11]. Our work on the programmable data protection device and secure programming manager has been the subject of **one European patent** application [P5-EU] in collaboration with STMicroelectronics, afterwards extended to **one US Patent granted in 2012** [P5-US].

Afterwards, secure monitoring services for NoCs have been presented in **CODES-ISSS-2008** [C36], while a run-time monitoring system based on NoCs has been proposed in **DATE-2009** [C34] and recently extended in the **IEEE Trans. on VLSI-2013** [J3]. Finally, I was also **Co-editor** of the scientific book: "Low-Power Networks-on-Chip" published by Springer in 2011 [E5].

2.1.6. Technology-aware Many-core Architectures Design

A basic tenet of my research is that power-aware application-specific many-core architectures must be tuned being aware of microarchitectural and technology problems and emphasizing the early-phase of design space exploration. Many challenging and relevant research topics related to many-core architectures are still open. There is still significant research to be done, and architectural and technology challenges will increase in importance as we scale down the fabrication process in the nanoscale era. I believe that technology-driven considerations (such as ultra-low-power design, resiliency and process variability) will further increase their importance on architecture and system level design in the next coming years. In the many-core era, system design optimization and exploration still represent challenging tasks. Networks-on-Chip, as an architectural solution for scalable high speed interconnect, and power-aware design will continue to be crucial topics, since power and energy issues still represent one of the limiting factors in integrating multi/many cores on a single chip. The power-wall problem and its dual utilization-wall problem are considered among the main barriers for an efficient performance scaling bringing to the **dark silicon** problem (where for dark silicon is intended the chip fraction not usable in a many-core chip due to the power budget). To address the dark silicon problem, **Near Threshold Computing (NTC)** has recently been proposed as a promising solution to mitigate the dark silicon effects by operating at lower frequency but exploiting a larger number of cores. However, NTC suffers from an increase sensitivity to technology problems (such as process variability).

In this context, I have recently opened a new research path in collaboration with Gianluca Palermo and Sotirios Xydis (Post-doc at National Technical University of Athens, formerly Post-doc at Politecnico di Milano) The main focus of our research is on **variability-aware NTC** architectures based on the formation of voltage islands with emphasis on voltage and workload allocation across the many-core architecture. We also introduced the usage of approximate computing concepts to sustain performance despite of variability effects.

Main achievements: Based on our former research work on variability-aware robust DSE for many-core architectures (published in **ASP-DAC-2009** [C35] and in **ACM Trans. on Embedded Computing Systems 2012** [J7]), our most recent achievement consists of a variability-aware framework based on fine-grained voltage islands for exploring the potential power-efficiency of NTC under performance constraints. The proposed approach will be presented next year in two high-impact venues: **ASP-DAC 2014** [C9] and **DATE 2014** [C6].

2.2. RESEARCH COLLABORATIONS

My research activities have been carried out in collaboration with several national and international universities (Università degli Studi di Bologna, Politecnico di Torino, Stanford University, ALaRI-Università della Svizzera Italiana, University of Cantabria, Technical University of Delft, Universidade Federal do Rio Grande do Sul), research centers (CEFRIEL (I), IMEC (B), Pacific Northwest National Laboratory (USA)) and ICT and semiconductor companies (Group Bull, IBM Research, STMicroelectronics, HP Labs, Intel, Siemens Mobile Communications). Among these collaborations we can mention:

1. **ALaRI** - Advanced Learning and Research Institute - Switzerland (2003 - Present) Contact Person: prof. M. Sami. Research topics: Design space exploration techniques based on response surface methods. Design and analysis of high level services for Network on-Chip architectures.
2. **IMEC** - Interuniversity Micro-Electronics Centre, Belgium (2007 - Present) Contact Persons: prof. Francky Catthor, Chantal Ykman Couvreur, Research topic: Design and analysis of an application-specific manager for power-aware adaptation.
3. **STMicroelectronics** - Agrate, Italy (1996 - Present) Contact Person: Dr. R. Zafalon. Research topics: Power estimation and optimization techniques for Network on-Chip architectures (1996 – 2006); Design space exploration of embedded computing architectures (2007 – Present).
4. **STMicroelectronics** - Grenoble, France (2005 - 2007) Contact Person: Dr. M. Coppola. Research topic: Design methodology and implementation of high-level services on the ST-NOC architecture.
5. **STMicroelectronics** - Grenoble, France (2010 - 2013) Contact Person: Dr. D. Melpignano. Research topic: Design

methodology and tools for many-cores computing fabrics.

6. **Fraunhofer - Heinrich Hertz Institut** – Berlin, Germany (2010 – 2013) Contact Person: Dr. Benno Stabernack. Research topics: Design space exploration od Scalable Video Coding applications
7. **NTUA** - National Technical University of Athens - Greece (2010 - Present) Contact Persons: prof. D. Soudris, Dr. S. Xydis. Research topics: Runtime management techniques for many-core architectures; Design and exploration of Near-Threshold Computing architectures.
8. **TUDelft** – Technical University Delft, The Nederlands (2008 - Present) Contact Person: prof. K. Bertels. Research topics: Design space exploration and run-time management techniques for reconfigurable computing platforms.
9. **PNNL** - Pacific Northwestern National Laboratory - WA, USA (2010 - Present) Contact Persons: Dr. A. Tumeo, Dr. O. Villa (currently at NVIDIA). Research topics: Design and analysis of a many-core/many-node architecture for irregular applications.
10. **UFRGS** - Universidade Federal do Rio Grande do Sul - Brazil (2009-Present) Contact Person: prof. L. Carro Research topic: Floorplan-aware design methodology for Network on-Chip architectures.
11. **IBM Research** - ASTRON & IBM Center for Exascale Technology, The Nederlands (2013 – Present) Contact Person: Dr. L. Fiorin. Research topic: Architectures and applications for exascale computing.
12. **UCI** - University of California at Irvine – CA, USA (2013 – Present) Contact Person: prof. Fadi Kurdahi. Research Topic: Near Threshold Computing for many-core architectures.

2.3. *COORDINATION OF EUROPEAN RESEARCH PROJECTS*

- **Project Coordinator of the European Project FP7-2PARMA-248716** on "PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures" (Jan. 2010 – Mar. 2013). http://www.2parma.eu/ EC Contribution to the project: 2.740 M€ funding. The 2PARMA Consortium was composed of seven partners: Politecnico di Milano (Italy), STMicroelectronics (Italy and France), Heinrich Hertz Institute - Fraunhofer Institute for Telecommunications (Germany), IMEC (Belgium), ICCS - Institute of Communication and Computer Systems (Greece), RWTH Aachen University (Germany), Synopsys (Belgium). The 2PARMA project focused on the definition of a parallel programming models, run-time resource management policies and design space exploration methodologies for many-core architectures. Applicability and benefits of the proposed techniques and tools have been validated and assessed on as set of industrial applications and hardware platforms. The 2PARMA project ended in March 2013 with an ***excellent evaluation*** by the European Commission demonstrating the fulfillment of its objectives and scientific/technical goals. Based on the opinion of the European expert reviewers: *"the project represents a **success story** and has made significant contributions to the state-of-the-art in the field".* Also the expected impact is considered to be ***excellent***. Finally the European expert reviewers commended me as Project Coordinator: *"for the efficiency and professionalism shown during the whole project; for demonstrating high management skills and strong leadership abilities and for establishing an efficient and effective collaboration amongst all the project partners".*
- **Project Coordinator of the European Project FP7-MULTICUBE-216693** on "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (Jan. 2008 - June 2010). http://www.multicube.eu/ EC Contribution to the project: 2.098 **M€** funding. The MULTICUBE Consortium was composed of nine partners: Politecnico di Milano (Italy), Design of Systems on Silicon – DS2 (Spain), STMicroelectronics (Italy), IMEC (Belgium), ESTECO (Italy), University of Lugano - ALaRI (Switzerland), University of Cantabria (Spain), STMicroelectronics Beijing (China), Institute of Computing Technology – Chinese Academy of Sciences (China). The MULTICUBE project finished in 2010 with an ***excellent evaluation*** by the EC demonstrating to fully achieve its objectives and scientific/technical goals. The project has demonstrated the benefits of using automated design exploration techniques (based on enhanced multi-objective optimization algorithms) by implementing a number of industrial use cases; practical ways to trade off accuracy for speed through the use of multi-abstraction level simulation thus enabling exploration of larger design spaces; the feasibility of automated parameter tuning at run-time using exploration data collected at design-time. Based on the opinion of the European expert reviewers, as Project Coordinator I've demonstrated "*high leadership capabilities and led very professionally all the management activities".* In the context of the MULTICUBE project, I was also leading a research group at Politecnico di Milano whose research focuses on design space exploration for multi-processor architectures working on an open-source tool **(MULTICUBE Explorer)** to enable an automatic and fast optimization of configurable system architectures towards a set of objective functions such as energy and delay.

2.4. *COORDINATION OF INDUSTRIAL FUNDED RESEARCH PROJECTS*

- **Principal Investigator (Responsabile Scientifico)** in the two-year research project: "Low Power Network on Chip and Multiprocessor Platforms" (2006-2008) between the Dipartimento di Elettronica e Informazione of Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics,** Agrate B.
- **Principal Investigator (Responsabile Scientifico)** in the two-year research project: "Low Power Network on Chip and Embedded Architectures" (2003-2005) between the Dipartimento di Elettronica e Informazione of Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics,** Agrate B.

2.5. PARTICIPATION TO EUROPEAN RESEARCH PROJECTS

- Participation to the recently started **European Integrated Project CONTREX - 611146** on "Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties" (Oct. 2013 – Sep. 2016). https://contrex.offis.de/home/ EC Contribution to the project: 6 050 Mio Euro. The CONTREX project includes fourteen partners from six countries. Project Coordinator: OFFIS (D). Local Principal Investigator: prof. W. Fornaciari.
- Participation to the recently started **European Project FP7-HARPA-612069** on "Harnessing Performance Variability" (Sep. 2013 – Aug. 2016). http://www.harpa-project.eu/ EC Contribution to the project: 2 797 Mio Euro. The HARPA project includes eight partners from six countries. Project Coordinator: prof. W. Fornaciari, Politecnico di Milano.
- Participation to the **ARTEMIS-2009-1-100230 SMECY Project** on "Smart Multicore Embedded Systems" (Feb. 2010 – Jan. 2013). http://www.smecy.eu The SMECY project includes thirty partners (among them STMicroelectronics and Thales) from nine European countries. Project Coordinator: Francois Pacull (CEA, France). Local Principal Investigator: prof. D. Sciuto.
- Participation to the **European Integrated Project COMPLEX - 247999** on "Co-design and power management in platform-based design space exploration" (Dec. 2009 – Feb. 2013). https://complex.offis.de/ EC Contribution to the project: 4.8 Mio Euro. The COMPLEX project included fourteen partners from six countries (including China). Project Coordinator: OFFIS (D). Local Principal Investigator: prof. W. Fornaciari.
- From 2006 to 2007, I collaborated as **Senior Researcher** with ALaRI-Advanced Learning and Research Institute, part of the Faculty of Informatics of the Università della Svizzera Italiana (CH) to the European research project **MEDEA+ LoMoSA+** (2A708): "Low-power expertise for Mobile & multi-media System Applications". Project Coordinator: NXP Semiconductors (NL). Local Principal Investigator: prof. M. Sami. The activity carried out in this project has been the subject of one European **patent application** [P5-EU], afterwards extended to the USA (**US patent** [P5-US] granted in 2012).
- Participation to the **European Project MEDEA+(A207) Pocket Multimedia** "Silicon application platform for pocket multimedia" (2001 – 2004). Project Coordinator: ST Microelectronics. Local Principal Investigator: Roberto Zafalon. In 2005, the project has won the annual award for European collaborative innovation in Microelectronics, the "Jean-Pierre Noblanc Award for Excellence."
- Participation to the **European Project FP6 - ICODES – 004452** "Interface and communication based design of embedded systems" (2004-2007). EC Contribution to the project: 2.850 Mio Euro. Project coordinator: OFFIS (D). Local Principal Investigator: prof. D. Sciuto.
- Participation to the **European Project FP6 – PEOPLE - 26796** "Power EstimatiOn for fast exPLoration of Embedded systems" funded by ESPRIT4-OMI (Open Microprocessor Initiative) from 1/4/1998 to 31/12/2000. Project coordinator: OFFIS (D). Local Principal Investigator: prof. D. Sciuto.

2.6. PARTICIPATION TO NATIONAL RESEARCH PROJECTS

- Two-year scientific national inter-university co-funded research program **MIUR – PRIN 2005** (Prot. 2005095528) "Metodologie di progettazione di sistemi multiprocessore on-chip basati sul concetto di piattaforma" (Design methodologies of multiprocessor systems-on-chip based on the concept of platform). National Scientific Coordinator: prof. D. Sciuto (Politecnico di Milano).
- Two-year scientific national inter-university co-funded research program **MIUR–2002** (Prot. 2002092153) "Metodologie di progetto per sistemi digitali integrati su singolo chip di tipo embedded" (Design methodologies for single-chip embedded systems). National Scientific Coordinator: prof. M. Sami (Politecnico di Milano)
- National scientific research project **FIRB – MAIS – 2001** "Sistemi informativi adattativi multicanale" (Adaptive multi-channel computing systems). National Scientific Coordinator: prof. B. Pernici (Politecnico di Milano).
- Two-year scientific national research project: **CNR Italian Research Council - 1997-98** Project: "Metodologie e Strumenti per la Progettazione Automatica di Circuiti e Sistemi Digitali a Basso Consumo di Potenza". (Methodologies and Tools for the Automatic Design of Low-Power Digital Circuits and Systems). National Scientific Coordinator: Prof. M. Mezzalama, Politecnico di Torino.

2.7. PARTICIPATION TO INDUSTRIAL FUNDED RESEARCH PROJECTS

- **Participation** to the two-year research project: "Power estimation methodologies for VLIW architectures" (2000-2002) between DEI - Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics,** Agrate B.. Principal Investigator: prof. M. Sami. The activity carried out in this project has been the subject of **one patent granted** by the USA Dept. of Commerce, Patent and trademark Office [P4-US].

2.8. EVALUATION OF RESEARCH PROJECTS FOR THE EUROPEAN COMMISSION:

1. **Independent Expert Reviewer,** ARTEMIS JU – Project 295440 PaPP (Portable and Predictable Performance on heterogeneous embedded many-cores), 2013-2015.
2. **Independent Expert Reviewer,** FP7 – STREP Project 288570 ParaPhrase (Parallel Patterns for Adaptive

Heterogeneous Multicore Systems), 2012-2014.

3. **Independent Expert Reviewer,** FP7 – STREP Project 248976 REFLECT (Rendering FPGAs to Multi-Core Embedded Computing), 2010-2012.
4. **Independent Expert Reviewer** to evaluate research proposals submitted to the "Future and Emerging Technologies" programme (EC FET-Open) on FP7-ICT-2009, 2010-2013.
5. **Independent Expert Reviewer** to participate in the on-site Evaluation Panel to evaluate research proposals submitted to the "Future and Emerging Technologies" programme (EC FET-Open) on FP7-ICT-2009 Batch 13, June 2012.
6. **Independent Expert Reviwer,** Network-of-Excellence Project FP6 - IST-4408 HiPEAC (High-Performance Embedded Architectures and Compilers) coordinated by prof. Mateo Valero, Universidad Politecnica de Catalunya, Barcelona. 2005-2008.
7. **Independent Expert Reviewer,** to participate to the on-site Evaluation Panel for the European IV Call IST (Information Society Technology) - FP6 (6th Framework Programme) on Nanoelectronics, April 2005.

2.9. EVALUATION OF RESEARCH PROJECTS FOR VARIOUS SCIENCE FOUNDATIONS

1. **Expert Reviewer,** Programme Blanc International Edition 2010, ANR (Agence Nationale de la Recherche), France, 2010.
2. **Chair of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering, 2009.
3. **Member of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering, 2008.
4. **Primary Evaluator**, INRIA (French National Institute for Computer Science - France), 2007..

3. SCIENTIFIC SERVICES

I'm an active member of the research community, and so far I've organized several international conferences and workshops as Program Chair or General Chair and I regularly serve in several technical program committees.

3.1. ORGANIZING COMMITTEE MEMBER

1. **Program Chair, FPL 2015,** 25th International Conference on Field Programmable Logic and Applications, to be held in London (UK), Sept., 2015.
2. **Subcommittee Chair, Embedded System Design, DAC 2015,** 52nd ACM/IEEE Design Automation Conference, San Francisco CA, June 7-11, 2015.
3. **Track Co-Chair, Architectural and Micro-architectural Design, DATE 2015,** IEEE/ACM Design and Test in Europe Conference, Grenoble (France), March 9-13, 2015.
4. **General Co-Chair, PARMA-DITAM Workshop 2015,** co-located with HiPEAC 2015 Conference, Amsterdam (NL), Jan. 19-21, 2015.
5. **Track Co-Chair, Design Methods and Tools, FPL 2014,** 24th International Conference on Field Programmable Logic and Applications, Munich (Germany), Sept., 2014.
6. **General Chair, PARMA-DITAM Workshop 2014**, co-located with HiPEAC Conference 2014, Wien (A), Jan. 20, 2014.
7. **Track Co-Chair, SoC Design and Interconnect, VLSI-SOC 2013,** 21st IFIP/IEEE International Conference on Very Large Scale Integration, Istanbul (Turkey), October, 2013.
8. **Workshops Co-Chair, FPL 2013,** 23rd International Conference on Field Programmable Logic and Applications, Porto, Sept. 2-4, 2013.
9. **General Co-Chair, DEPCP 2013,** 5th DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 22nd, 2013.
10. **General Co-Chair, Fall School** on Programming Paradigms for Multi-core Embedded Systems, Freudenstadt – Lauterbad, Germany, October 2-5, 2012.
11. **Program Co-Chair, ASAP 2012,** 23rd IEEE International Conference on Application-specific Systems, Architectures and Processors, Delft (NL), 9-11 July 2012.
12. **Subcommitte Co-Chair, Embedded Systems Design Methodologies, DAC 2012,** ACM/IEEE Design Automation Conference, San Francisco CA, 3-7 June 2012.
13. **General Co-Chair, DEPCP 2012,** 4th DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 16th, 2012.
14. **Co-Organizer, RAPIDO Workshop 2012** on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2012, Paris.
15. **General Co-Chair, DEPCP 2011,** 3rd DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 18th, 2011.
16. **Program Co-Chair, ARCS 2011,** Architecture of Computing Systems Conference, Como (Italy), 22-25 Feb. 2011.
17. **Co-Organizer, RAPIDO Workshop 2011,** on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2011, Crete.
18. **Top Picks 2010, Selection Committee Member, IEEE MICRO Special Issue** on "Top Picks 2010 from Computer Architecture Conferences", January/February 2011.
19. **Program Co-Chair, SASP 2010,** IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference), Anaheim, CA, June 13-18, 2010.
20. **Co-Organizer and Architectures Session Chair, DEPCP 2010,** Second DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 12th, 2010.
21. **General Co-Chair, PARMA Workshop 2010** on Parallel Programming and Run-time Management Techniques for Many-core Architectures, co-located with ARCS 2010 - Architecture of Computing Systems Conference, Hannover (D), February 2010.
22. **Co-Organizer, RAPIDO Workshop 2010** on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2010, Pisa.
23. **General Co-Chair, SASP 2009,** IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) San Francisco, CA, July 27-28, 2009.
24. **Program Co-Chair, SAMOS IX Workshop** on Systems, Architectures, Modeling and Simulation, Samos, Greece, July, 2009.
25. **Co-Organizer and Architectures Session Chair, DEPCP 2009,** First DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Nice, April 24th, 2009.
26. **General Co-Chair, MICRO 2008,** 41st Annual IEEE/ACM International Symposium on Microarchitecture, Como (Italy), 8-12 November 2008.

27. **Publicity Chair, SASP 2008,** IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) Anaheim, CA, June 8-9, 2008.
28. **Publicity Chair, WASP2007,** Fifth Workshop on Application Specific Processors, 2007.

3.2. PROGRAM COMMITTEE MEMBER

1. **IPDPS,** IEEE International Parallel and Distributed Processing Symposium, 2015.
2. **DAC,** ACM/IEEE Design Automation Conference, 2011-2013, 2015.
3. **DATE,** IEEE/ACM Design and Test in Europe Conference, 2005-2015.
4. **FPL,** International Conference on Field Programmable Logic and Applications, 2013-2015.
5. **ICCAD,** IEEE/ACM International Conference on Computer-Aided Design, 2014.
6. **NOCS,** ACM/IEEE International Symposium on Networks-on-Chip, 2009-2014.
7. **DSD,** Euromicro Conference on Digital System Design, 2012- 2014.
8. **ASAP,** IEEE International Conference on Application-specific Systems, Architectures and Processors**,** 2012-2014.
9. **ARCS,** Architecture of Computing Systems Conference, 2010-2014.
10. **IC-SAMOS,** International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2006-2014.
11. **HPCC,** IEEE International Conference on High Performance Computing and Communications, 2014.
12. **ICPP,** IEEE International Conference on Parallel Processing, 2011, 2013.
13. **EUC 2013,** IEEE/IFIP Int. Conf. on Embedded and Ubiquitous Computing, 2013.
14. **MES 2013,** International Workshop on Many-core Embedded Systems.
15. **VLSI-SOC,** IFIP/IEEE International Conference on Very Large Scale Integration, 2008-2011, 2013.
16. **HPCA-18,** The 18th International Symposium on High Performance Computer Architecture, 2012.
17. **IA^3,** Workshop on irregular Applications: Architectures and Algorithms, 2011-2012
18. **CF,** ACM International Conference on Computing Frontiers, 2009, 2012.
19. **WRC,** Workshop on Reconfigurable Computing, co-located with HiPEAC Conference, 2010-2012.
20. **PDP,** Euromicro International Conference on Parallel, Distributed and Network-Based Computing, 2012
21. **SASP,** IEEE Symposium on Application Specific Processors, 2008-2011.
22. **MICRO-43,** 43rd Annual IEEE/ACM International Symposium on Microarchitecture, 2010.
23. **HiPEAC,** International Conference on High-Performance Embedded Architectures and Compilers, 2010.
24. **ICS,** the 20th ACM International Conference on Supercomputing, 2006.
25. **WASP,** Workshop on Application Specific Processors, 2004-2007.

3.3. ASSOCIATE/GUEST EDITOR AND JOURNAL REVIEWER

- **Associate Editor MICPRO Journal,** Embedded Hardware Design (Microprocessor and Microsystems), Elsevier (2013- now)
- **Guest Co-Editor,** Special Issue DSD2012 on Reliability and Dependability in MPSoC Technologies, Journal on Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), Elsevier, Vol. 37, Number 8-A, 2013 (09/2012 – 12/2012)
- **Guest Co-Editor,** Special Issue with selected papers from International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS2009) on Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), Volume 5, Issue 3, Springer. (09/2009 – 03/2010)
- **Subject Area Editor,** Journal of Systems Architecture – The EUROMICRO Journal, Elsevier Ed. (06/2003 - 10/2005).
- Since 1993 to present, I'm servicing as **reviewers** for several prestigious international journals such as: IEEE Transactions on Computers; IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems; IEEE Transactions on Very Large Scale Integration Systems; IEEE Design and Test; IEEE Micro; ACM Transactions on Design Automation of Electronic Systems; ACM Transactions on Embedded Computing Systems; Springer Journal on VLSI Signal Processing Systems; Springer Journal on Design Automation for Embedded Systems; Elsevier Journal on Microprocessors and Microsystems: Embedded Hardware Design (MICPRO); IET Computers and Digital Techniques;

3.4. INVITED TALKS, SEMINARS AND PANELS

1. October 8th, 2014, "Managing Adaptability in Heterogeneous Architectures through Performance Monitoring and Prediction", **Invited Talk** at the Thematic Section on Heterogeneous System Tools for Simulation, Debugging, Performance Modeling and Resource Management, HiPEAC Computing System Week, Athens, Host: Prof. Georgios Goumas, National Technical University of Athens.
2. May 15th, 2014, "Managing Adaptability in Dynamically Reconfigurable Architectures through Performance Monitoring and Prediction", **Invited Talk** at the Thematic Section on Reconfigurable Computing, HiPEAC Computing System Week, Barcelona, Host: Prof. Georgi Gaydadjiev, Chalmers University of Technology.
3. September 4th, 2013, **Panel Moderator** on: "EU Horizon 2020 on Reconfigurable Computing" Invited Speakers: Dr. Panos Tsarchopoulos, Future and Emerging Technologies, EU Project Officer; Dr. Georgi Kuzmanov, ARTEMIS Joint Undertaking, EU Programme Officer; held at FPL2013, 23rd International Conference on Field Programmable Logic and Applications, Porto.
4. June 8th, 2012, "Automatic Design Space Exploration for Multi-core Architectures", **Seminar** at Intel Labs, Santa Clara (CA, USA), Host: Dr. Akhilesh Kumar, Intel.
5. April 25th, 2012. "Design-time support for run-time management of embedded multiprocessor architectures", **Invited Talk** at the Thematic Section on Design and runtime management of reconfigurable systems, HiPEAC Computing System Week, Goteborg, Host: Prof. Georgi Gaydadjiev, Chalmers University of Technology.
6. February 7th, 2012, "Design Space Exploration and Run-time Resource Management for Multi-core Architectures", **Seminar** at the University of Texas at Austin, Electrical and Computer Engineering, Computer Architecture Seminar Series, Austin, Host: Prof. Yale Patt, University of Texas at Austin.
7. September 7th, 2011, "2PARMA Project" **Invited Talk** at FPL2011 European Project Workshop, Chania, Crete. Organizer. Prof. Joao Cardoso, Univ. of Porto.
8. April 7th, 2011, "2PARMA Project: PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures", **Invited Talk,** HIPEAC Cluster Meeting on Multi-core Architectures, 2011 Chamonix (F), Host: Prof. Per Stenström, Chalmers University of Technology.
9. November 24th, 2010, "Automatic Design Space Exploration for Chip Multi-processors", **Invited Talk** at the Workshop on "Challenges in Embedded System Design": Involvement of SMEs in Designing Complex Systems (CMM 2010), University of Lugano, Switzerland, Workshop Organizers: Prof. G. De Micheli (EPFL) and Prof. M. Sami (USI-Politecnico di Milano).
10. July 6th, 2010, "MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures", **Invited Talk** at the Research Projects Workshop at ISVLSI 2010: IEEE Computer Society Annual Symposium on VLSI, July 5-7, 2010, Lixouri Kefalonia, Greece.
11. June 18th, 2010, "Automatic Design Space Exploration for Chip-Multi Processors". **Seminar** at University of California Riverside, Department of Computer Science & Engineering, Riverside (CA, USA), Host: Prof. Walid Najjar, University of California Riverside.
12. June 17th, 2010, "Automatic Design Space Exploration for Chip-Multi Processors". **Seminar** at University of California Irvine, Department of Computer Science & Engineering, Irvine (CA, USA), Host: Prof. Alexander V. Veidenbaum, University of California Irvine.
13. March 23rd, 2010, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "A Design Space Exploration Framework for Run-Time Resource Management on Multi-Core Architectures" . Host: Prof. Koen Bertels, Delft Technical University.
14. December 17th, 2009, **Seminar** at NEC Laboratories America, Inc., Princeton Campus, Princeton (NJ - USA), Title: "Automatic Design Space Exploration for Chip-Multi Processors". Host: Dr. Marcello Lajolo, NEC Labs America.
15. December 16th, 2009, **Seminar** at Princeton University, Department of Electrical Engineering, Computer Engineering Seminar, Title: "Automatic Design Space Exploration for Chip-Multi Processors", Host: Prof. Ruby Lee, Princeton University.
16. July 29th, 2009, **Seminar** at HP Labs, Palo Alto, Title: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs", Host: Dr. Matteo Monchiero, HP Labs, Palo Alto.
17. May 14th, 2009, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs" Host: Prof. Koen Bertels, Delft Technical University.
18. April 25th, 2006, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "Exploration and Optimization of Multiprocessor Embedded Architectures based on Networks-on-Chip", Host: Prof. Stamatis Vassiliadis, Delft Technical University.
19. September 22nd, 2005, New York, USA, **Panelist at WASP 2005** Workshop on Application Specific Processors (co-

located with International Conference on Hardware/Software Codesign and System Synthesis), Panel title: "Application Specific Customizations: Processor or System Level?" Moderator: Prof. Daniel Gajski, UC Irvine.

3.5. MEMBER OF PROFESSIONAL ORGANIZATIONS

- Since 2013, **Member** of ACM (Association of Computing Machinery).
- Since 1993, **Member** of IEEE (Institute of Electrical and Electronics Engineers) and **Senior Member** since August 2009.
- Since 2008, **Member** of HiPEAC Network of Excellence.

4. ACADEMIC SERVICES

4.1. TEACHING ACTIVITIES AT UNIVERSITIES

With respect to teaching, I have balanced my efforts in the past years in teaching both at the Undergraduate level and at the Master of Science level at Politecnico di Milano and previously at the Università degli Studi di Milano. At the Undergraduate level, I have covered several courses in the Computer Engineering track: Computer Architectures, Operating Systems, Logic Design and Computer Science Fundamentals. At the M. Sc. level, I have taught courses mainly related to my research areas: Advanced Computer Architectures and Hardware/Software Co-design Methodologies. I have an extensive **English-speaking teaching experience** in a multicultural environment thanks to my courses at the M.Sc. program in Computer Engineering at the Como Campus of Politecnico di Milano (2003-present) and at the Università della Svizzera Italiana (2012). From 2002 to present, I was **advisor of about 60 M.Sc. students** in Computer Engineering at Politecnico di Milano. Since 20002, I was member of several Thesis Committees at the Undergraduate and M. Sc. level in Computer Engineering at Politecnico di Milano. Apart from course developments, **I enjoy teaching and I have a strong commitment to teach topics related to Computer Architectures.** My efforts are devoted to directly transfer to the students my research knowledge and results not only through continuously updating the concepts exposed in the courses to reflect state-of-the-art concepts, but also during the advising of the students for the development of course projects and M.Sc. thesis. This process is to make sure the students are aware of the state-of-the-art research on computer architectures and related tools. It is also important to have a constructive and continuous interaction with the students and to allow them to contribute to the improvements and quality assessment in teaching. I believe top quality teaching and good international visibility are key issues to guarantee adequate levels of in-flow of high quality students. A way to enhance the industrial exposure of our M.Sc. students is by offering internships during which they can work on industrial projects. In the past years, I have followed several students doing an internship (in the context of their Master thesis) with STMicroelectronics. Furthermore, I'm **co-author of the academic textbook** (in Italian): "Progettazione digitale" (Logic Design) edited by McGraw-Hill, First Edition 2002, Second Edition 2007. The textbook has been written to be used at the undergraduate level in basic courses of Logic Design in Computer Engineering and Computer Science tracks.

2014/2015

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2015.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus (Course completely offered in English) , Spring 2015.

2013/2014

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English) , Spring 2014
- "Architettura dei Calcolatori e Sistemi Operativi (I Modulo)" (5 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, , Fall 2013.
- "Architetture Avanzate dei Calcolatori" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2013.

2012/2013

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2013.
- "Architettura dei Calcolatori e Sistemi Operativi (I Modulo)" (5 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2012.
- "Advanced Computer Architectures" (3 Credits), Master of Science, Embedded System Design, Università della Svizzera Italiana, Lugano (Course completely offered in English), Fall 2012.

2011/2012

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2012.
- "Architettura dei Calcolatori e Sistemi Operativi" (10 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2011.

2010/2011

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2011.
- "Architettura dei Calcolatori e Sistemi Operativi" (10 Ccredits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2010.

2009/2010

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2010.
- "Architettura dei Calcolatori e Sistemi Operativi" (10 Credits), Undergraduate Programme, Computer Engineering,

Politecnico di Milano, Como Campus, Fall 2009.

2008/2009

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2009.
- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2008.

2007/2008

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2008
- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2007.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2007.

2006/2007

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2007.
- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2006.
- "Informatica A " (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2006.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2007.
- "Advanced Computer Architectures", (2.5 Credits) Ph. D. Programme, Computing Systems Engineering, Politecnico di Milano, Milano Leonardo Campus (in collaboration with prof. M. Sami), Spring 2007.

2005/2006

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2006.
- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2005.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2005.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2006.

2004/2005

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus, Spring 2005.
- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2004.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2004.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2005.

2003/2004

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus, Spring 2004.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2003.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2004.

2002/2003

- "Calcolatori Elettronici" (10 Credits), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2003.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2002.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2003.

2001/2002

- "Calcolatori Elettronici" (10 Credits), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2002.

- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2002.
- "Computer Architectures I" (Labs for prof. N. Scarabottolo), Undergraduate Programme, Computer Science, University of Milan, Crema Campus, Fall 2001.

2000/2001

- "Architettura degli Elaboratori I" (Labs for prof. N. Scarabottolo), Undergraduate Programme, Computer Science, University of Milan, Crema Campus, Fall 2000.
- "Architettura degli Elaboratori e delle Reti / II Modulo" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Spring 2001.
- "Laboratorio di Sistemi Operativi / I Modulo" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Spring 2001.
- "Advanced Computer Architectures" (3 Credits), Ph. D. Programme, Computer Science, Department of Computer Science, University of Milan, Spring 2001.
- "Calcolatori Elettronici" (Labs for prof. M. Sami), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2001.

1999/2000

- "Laboratorio di Architettura degli Elaboratori I" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Crema Campus, Fall 1999.
- "Calcolatori Elettronici" (Labs for prof. M. Sami), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2000.
- "Calcolatori Elettronici" (Labs for prof. R. Stefanelli), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2000.

4.2. *ACADEMIC RESPONSIBILITIES*

Since 2002, I am an active and permanent contributor to the organisation of the teaching activities and tracks in Computer Engineering at Politecnico di Milano, Como Campus, where I have had several responsibilities and I was participating to a number of committees:

- ***Chair,*** Committee on Undergraduate Study Plans (Commissione Piani degli Studi Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2002-Present.
- ***Chair,*** Committee on Undergraduate Transfers (Commissione Passaggi e Trasferimenti Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- ***Member,*** Committee on Graduate Admissions (Commissione Ammissioni alla Laurea Magistrale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- ***Member,*** Committee on Undergaduate Studies (Commissione Didattica Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.

After the recent merging of the organisation of Computer Engineering tracks in Como Campus and Milano Leonardo Campus, I have started to collaborate to the following committee:

- ***Member,*** Committee on Studies (Commissione Didattica) in Computer Engineer, Politecnico di Milano, Sept. 2013-Present.
- ***Member,*** Committee on Graduate Admissions (Commissione Ammmissioni alla Laurea Magistrale), School of Industrial and Information Engineering, Politecnico di Milano, May 2013-Present.

I have also been part of the following temporary committees:

- ***Member,*** Committee for the comparative evaluation of the candidates for the position of Temporary Researcher (Ricercatore Temporaneo) in Computer Engineering , Politecnico di Milano, 2010.
- ***Member,*** Committee for the comparative evaluation of the candidates for one position as Assistant Professor (Ricercatore MIUR) in Computer Engineering , University of Catania, 2007-2008.

4.3. *RESEARCH ADVISING*

4.3.1. *Doctoral Students Supervision*

1. **Vittorio Zaccaria,** Ph. D. 2002, Politecnico di Milano. Currently Assistant Professor at Politecnico di Milano, DEIB. First employment: R&D Engineer at STMicroelectronics. Ph.D. Thesis on: "Power exploration methodologies for VLIW-based systems", Advisor: prof. M. Sami. Co-advisors: prof. D. Sciuto, Dr. C. Silvano.
2. **Gianluca Palermo,** Ph.D. 2006, Politecnico di Milano. Currently Assistant Professor at Politecnico di Milano, DEIB. First employment: Post-Doctoral Researcher at Politecnico di Milano. Ph.D. Thesis on: "Design Methodologies for Embedded Architectures based on Network on-Chip", Advisor: prof. C. Silvano.
3. **Giovanni Beltrame,** Ph.D. 2006, Politecnico di Milano. Currently Assistant Professor at École Polytechnique de Montréal. First employment: Microelectronics Engineer at European Space Agency (NL). Ph.D. Thesis on "Modeling, Simulating, Analysis and Optimization of Multi-Processor System-on-Chip Platforms", Advisor: prof. D. Sciuto. Co-advisor: prof. C. Silvano.
4. **Matteo Monchiero,** Ph.D. 2007, Politecnico di Milano. Currently Senior Research Scientist, Intel Labs at Santa Clara

(CA, US). First employment: Post-Doctoral Research Associate at HP Labs in Palo Alto, Exascale Computing Lab., Ph.D. Thesis on: "Power/performance analysis and optimization of multicore architectures", Advisor: prof. C. Silvano.

5. **Oreste Villa,** Ph.D. 2008, Politecnico di Milano. Currently Senior Research Scientist, at NVIDIA (CA). First employment: Research Scientist at Pacific Northwest National Laboratory , Richland, WA (USA), Ph.D. Thesis: "Designing and Programming Multi-core Architectures", Advisor: prof. C. Silvano.
6. **Giovanni Mariani,** Ph. D. 2011, Università della Svizzera Italiana (USI). Currently Post-Doctoral Researcher at ASTRON & IBM Center of Exascale Technology (NL). First employment Post-Doc at ALaRI - USI (CH) and Associate Researcher at TU Delft(NL). Ph.D. Thesis: "A Design Space Exploration Methodology Supporting Run-time Resource Management for Multi-Core Architectures", Advisor: prof. M. Sami, Co-advisor: prof. C. Silvano
7. **Leandro Fiorin,** Ph. D. 2012, Università della Svizzera Italiana (USI). Currently Post-Doctoral Researcher at ASTRON & IBM Center for Exascale Technology (NL). First employment: Post-Doc at ALaRI –USI (CH). Ph.D. Thesis: "High level services for Networks-on-Chip", Advisor: prof. M. Sami, Co-advisor: prof. C. Silvano.
8. **Edoardo Paone,** Ph. D. student at Politecnico di Milano, DEIB, XXVII cycle. Ph.D. Thesis: "Design Space Exploration of OpenCL Applications on Heterogeneous Parallel Platform". Ph.D. defense expected Dec. 2014. Advisor: prof. C. Silvano.
9. **Ioannis Stamelakos,** Ph. D. student at Politecnico di Milano, DEIB, XXVIII cycle. Ph.D. Thesis: "Technology-Aware Many-core Architecture Design". Ph.D. defense expected 2016. Advisor: prof. C. Silvano. Co-advisor: prof. G. Palermo.
10. **Amir Hossein Ashouri,** Ph. D. student at Politecnico di Milano, DEIB, XXVIII cycle. Ph.D. Thesis: "Compiler/Architecture Co-exploration of Customized VLIW Architectures". Ph.D. defense expected 2016. Advisor: prof. C. Silvano.
11. **Davide Gadioli,** Ph. D. student at Politecnico di Milano, DEIB, XXIX cycle. Ph.D. Thesis: "Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications". Ph.D. defense expected 2017. Advisor: prof. C. Silvano. Co-advisor: prof. G. Palermo.

4.3.2. Undergraduate and Master Students Supervision

- Advisor of more than **60** Master students in Computer Engineering, Electrical Engineering, and Communication Engineering at Politecnico di Milano, 2002-Present.
- Advisor of some undergraduate and Master students in Computer Science at Università degli Studi di Milano, 2000-2002.
- Co-advisor of some Master students in Electrical Engineering at Università degli Studi di Brescia, 1996-1999.
- Advisor / co-advisor of some Master students in Information Technology at CEFRIEL Research and Training Center in Milano, EDA (Electronic Design Automation) Group, 1993-1999.

4.4. PHD EXTERNAL EXAMINER

- In November 2014, I have been invited as Opponent Member of the Doctoral Examination Committee, Eindhoevn University of Technology (NL), for the Ph.D. defense of the candidate **Dongrui She** discussing a thesis titled: "Energy Efficient Code Genertion for Streaming Applications", Advisors: prof. Henk Corporaal.
- In June 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, Technical University of Catalonia (Spain) for the Ph.D. defense of the candidate **Friman Sánchez Castaño** discussing a thesis titled: "Exploiting Multiple Levels of Parallelism in Bioinformatics Applications", Advisors: prof. Alex Ramírez and prof. Mateo Valero.
- In April 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, University of Verona, for the Ph. D. defense of the candidate **Francesco Stefanni** discussing a thesis titled: "A design and verification methodology for networked embedded systems", Advisor: prof. Franco Fummi.
- In February 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate **Kamana Sigdel** discussing a thesis titled: "System-level Design Space Exploration of Reconfigurable Architectures". Advisors: prof. K. Bertels and prof. A. Pimentel.
- In May 2009, I have been invited as Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate **Carlo Galuzzi** discussing a thesis titled: "Automatically fused instructions". Advisor: prof. K. Bertels.

4.5. VISITORS

1. **Sotirios Xydis, Ph.D.,** currently Post-Doctoral Researcher at National Technical University of Athens; **Post-Doctoral Researcher** in my group at Politecnico di Milano (From Nov. 2011 to July 2013). His current research focuses on design space exploration, high level synthesis and programmable architectures
2. Arpad Gellért, Ph. D., Assistant Professor, "Lucian Blaga" University of Sibiu, Romania, Advisor: Prof. Lucian Vintan. **Visiting Researcher,** Spring 2009.
3. **Caroline Concatto,** Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 15-01-10 to 15-04-10 , FP7 HiPEAC NoE Collaboration Grant.

4. **Debora Matos,** Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 02-02-11 al 02-05-11, FP7 HiPEAC NoE Collaboration Grant.
5. **Anelise Kologeski,** Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 02-02-11 al 02-05-11, FP7 HiPEAC NoE Collaboration Grant.

5. LIST OF PATENTS AND AWARDS

5.1. PATENTS

Inventor/Co-inventor of **11** patent applications with Bull HN Information Systems and STMicroelectronics **(7 out of 11 already granted)**:

- Integrated CMOS static RAM, EU Patent # **EP0578900 (B1)** [P1-EU] Granted 1997, DE Patent # **DE69223046 (T2)** [P1-DE] Granted 1998. Applicant: Bul HN Information Systems (IT)
- Digital information error correcting apparatus for single error correcting (SEC), double error detecting (DED), single byte error detecting (SBED), and odd numbered single byte error correcting (OSBEC), US Patent # **US5535227 (A)** [P2-US] Granted 1996. EU Patent # **EP0629051 (B1)** [P2-EU] Granted 1998, DE Patent # **DE69317766 (T2)** [P2-DE] Granted 1998. Applicant: Bul HN Information Systems (IT).
- Encoder/decoder architecture and related processing system, US Patent # **US20020019896 (A1)** [P3-US] Filed 2002. Encoder architecture for parallel busses, EU Patent # **EP1150467 (A1)** [P3-EU] Filed 2001. Applicant: ST Microelectronics (IT)
- Processor architecture US Patent # **US6889317 (B2)** [P4-US] Granted 2005. Processor architecture with variable-stage pipeline, EU Patent # **EP1199629 (A1)** [P4-EU] Filed 2002. Applicant: ST Microelectronics (IT)
- Programmable data protection device, secure programming manager system and process for controlling access to an interconnect network for an integrated circuit. US Patent # **US8185934 (B2)** [P5-US] Granted 2012. EU Patent # **EP2043324 (A1)** [P5-EU] Filed 2009. Applicant: STMicroelectronics Grenoble (F)

5.2. AWARDS

- **HiPEAC 2010 Paper Award,** given by the Steering Committee of the HiPEAC Network of Excellence as co-author of the paper: "A Correlation-Based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip " by G. Mariani, G. Palermo, V. Zaccaria, A. Brankovic, J. Jovic, C. Silvano. In Proceedings of **DAC-47** - Design Automation Conference, Anaheim, CA, USA, June 2010, pp. 120-125 url: http://www.hipeac.net/award
- In 2008, the paper "Address Bus Encoding Techniques for System-Level Power Optimization", by L. Benini, G. De Micheli, E. Macii, D. Sciuto, C. Silvano, DATE-98 has been recognized as one of the **most influential papers** of the past ten years DATE and then selected to be re-published as a chapter of the volume: **Design, Automation, and Test in Europe - The Most Influential Papers of 10 Years DATE** Lauwereins, Rudy; Madsen, Jan (Eds.), 2008.
- **ACM Recognition of Service Award,** given in Appreciation for Contributions to ACM as General Co-Chair MICRO-41: The 41st Annual IEEE/ACM Int. Symposium on Microarchitecture, Nov. 8-12, 2008.
- **Best Paper Award SAC 2008,** given at the 23rd Annual ACM Symposium on Applied Computing (Applications Theme) as co-author of the paper: M. Sykora, G. Agosta e C. Silvano, "Dynamic Configuration of Application Specific Implicit Instructions for Embedded Pipelined Processors", Fortaleza, Brazil, 16-20 March, 2008.
- **Bull Technical Award 1991**, given by Bull HN Information Systems for my contribution to the project: *"Integrated CAD framework for complex ASIC design"*. The award has been motivated by my contribution to the solution to relevant technical problems demonstrating high professional competences, originality approach and constant personal commitment.

6. LIST OF PUBLICATIONS

6.1. INTERNATIONAL JOURNALS WITH PEER REVIEW

2014

[J1]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "DeSpErate++: An Enhanced Design Space Exploration Framework using Predictive Simulation Scheduling", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Accepted for publication, 2014.**

[J2]. Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High Level Synthesis", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Accepted for publication, 2014.**

[J3]. Leandro Fiorin, Gianluca Palermo and Cristina Silvano. "A Configurable Monitoring Infrastructure for NoC-Based Architectures", IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol. 22, No. 11, November 2014, pp. 2436-2440, DOI: 10.1109/TVLSI.2013.2290102

2013

[J4]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "Design Space Exploration and Run-time Resource Management for Multi-cores", **ACM Transactions on Embedded Computing Systems (TECS),** Vol. 13, Issue 2, Special Issue on Application Specific Processors, September 2013, pp. 20:1-20:27 DOI = 10.1145/2520000.2514647

[J5]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "ARTE: An Application-specific Run-Time managEment framework for multi-cores based on queuing models", **Parallel Computing, Elsevier Journal,** Vol. 39, Issue 9, September 2013, pp. 504-519 Available online 20 April 2013, ISSN 0167-8191, DOI: 10.1016/j.parco.2013.04.002

2012

[J6]. Andrea Di Biagio, Giovanni Agosta, Cristina Silvano and Martino Sykora, "Architecture Optimization of Application-Specific Implicit Instructions". **ACM Transactions on Embedded Computing Systems (TECS),** Vol. 11, Issue S2, Article No. 44 (August 2012), pages 44:1 --44:23 (23 pages), DOI=10.1145/2331147.2331154

[J7]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria, "A Variability-Aware Robust Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints". **ACM Transactions on Embedded Computing Systems (TECS),** Vol. 11, Issue 2, Article 29 (July 2012), pages 29:1 --29:28 (28 pages). DOI=10.1145/2220336.2220341

[J8]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Space", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 31, No. 5, May 2012, pp. 740-753, DOI: 10.1109/TCAD.2011.2177457

2011

[J9]. Chantal Ykman-Couvreur, Prabhat Avasare, Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Linking run-time resource management of embedded multi-core platforms with automated design-time exploration", **IET Computers and Digital Techniques,** March 2011, Vol. 5, Issue 2, pp. 123-135 DOI: 10.1049/iet-cdt.2010.0030

2009

[J10]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "ReSPIR: A Response Surface-Based Pareto Iterative Refinement for Application-Specific Design Space Exploration", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 28, No. 12, Dec. 2009, pp. 1816-1829, DOI: 10.1109/TCAD.2009.2028681

2008

[J11]. Leandro Fiorin, Gianluca Palermo, Slobodan Lukovic, Valerio Catalano, Cristina Silvano, "Secure Memory Accesses on Networks-on-Chip", **IEEE Transactions on Computers,** Vol. 57, No. 9, pp. 1216-1229, Sept., 2008, ISSN: 0018-9340, DOI: 10.1109/TC.2008.69

2007

[J12]. Giovanni Beltrame, Donatella Sciuto, Cristina Silvano, "Multi-Accuracy Power and Performance Transaction-Level Modeling", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Volume: 26, No. 10, October 2007, Pages: 1830 -1842, DOI: 10.1109/TCAD.2007.895790

[J13]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors", **Journal of Systems Architecture: The Euromicro Journal** - Elsevier, Volume 53, Number 10, October 2007, pp. 719-732, DOI: 10.1016/j.sysarc.2007.01.008

[J14]. Cristina Silvano, Giovanni Agosta, Gianluca Palermo, "Efficient Architecture/Compiler Co-Exploration Using Analytical Models", **Design Automation for Embedded Systems,** Springer, Volume 11, Issue 1, March 2007, pp. 1-23, ISSN 0929-5585 (Print) 1572-8080 (Online), DOI: 10.1007/s10617-006-9588-7, url http://dx.doi.org/10.1007/s10617-006-9588-7

2006

[J15]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Efficient Synchronization for Embedded on-Chip Multiprocessors", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems,** Vol. 14, No. 10, October 2006, pp. 1049-1062, DOI 10.1109/TVLSI.2006.884147

2005

[J16]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "An Efficient Synchronization Technique for Multiprocessor Systems on-Chip". **ACM SIGARCH Computer Architecture News** (ACM, New York, USA) Volume 34, Issue 1 (March 2006) pp. 33-40. ISSN: 0163-5964, Special Issue on MEDEA-05 - International Workshop on MEmory performance: DEaling with Applications, systems and architecture" DOI 10.1145/1147349.1147357

[J17]. Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria, "Multi-Objective Design Space Exploration of Embedded Systems", **Journal of Embedded Computing, IOS Press,** Vol. 1, No. 3, 2005, pp. 305-316, ISSN 1740-4460, url

[J18]. Andrea Bona, Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Reducing the Complexity of Instruction-Level Power Models for VLIW Processors", **Design Automation for Embedded Systems,** Springer US, March 2005, Vol. 10, No. 1, pp. 49-67, DOI: 10.1007/s10617-006-9045-5

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