

CV SUMMARY - CRISTINA SILVANO

I am currently **Associate Professor (with tenure)** of Computer Engineering at [Politecnico di Milano](#) (Dip. di Elettronica, Informazione e Bioingegneria). In December 2013, I received the Scientific National Qualification in Italy as **Full Professor** in sector 09/H1 Information Processing Systems and 01/B1 Informatics. I have recently been named **IEEE Fellow** (effective from 2017) by the IEEE Boards of Directors “for contributions to energy-efficient computer architectures”.

RESEARCH ACTIVITIES

My current research focuses on **Computer Architectures** and **Electronic Design Automation**, with emphasis on power-aware design, design space exploration of embedded architectures, application autotuning for many-core architectures, Network-on-Chip architectures and technology-aware many-core architectures.

RESEARCH PROJECTS AND INTERNATIONAL COLLABORATIONS

My research activities have been carried out in collaboration with several international universities, research centers and industries (about **100** out of my **160** scientific publications include co-authors with different affiliations, **40** out of them with industrial co-authors, **120** co-authors overall). My research has been funded by several national and EU projects selected based on a competitive process. Among them, I am currently **Project Coordinator** of the H2020-FET-HPC European project [ANTAREX](#) (2015-2018) on “AutoTuning and Adaptivity approach for Energy efficient eXascale HPC systems”. Previously, I was **Project Coordinator** of two European projects: [FP7-2PARMA](#) (2010-2013) and [FP7-MULTICUBE](#) (2008-2010). Since 1996, I have started a continuous research collaboration with **STMicroelectronics** on power-aware embedded architectures. I was **Principal Investigator** of two industrial research projects funded by STMicroelectronics (2003-2008). Finally, I have been nominated **Project Manager** of the **IBM/POLIMI Collaborative Innovation Center on Big Data Analytics** (2015-Present).

SCIENTIFIC OUTCOMES

My scientific production consists of [more than 160 publications](#):

- Co-author of **28** top-ranked journal publications including **17 IEEE/ACM Transactions**: **6** IEEE Trans. on CAD, **5** IEEE Trans. on VLSI Systems, **3** ACM Trans. on Embedded Computing Systems, **1** IEEE Trans. on Architecture and Compiler Optimization, **1** IEEE Trans. on Computers, **1** IEEE Trans. on Information Theory;
- Co-author of more than **90** scientific publications on peer-reviewed conferences/workshops including **top-level conferences** (**20** DATE, **8** CODES-ISSS, **3** ASP-DAC, **2** DAC, **2** CASES and **1** ICCAD) collecting one Best Paper Award, one HiPEAC paper award and one of the most influential papers published at DATE conference in the decade 1998-2008;
- Co-editor of **4** Special Issues and **3** scientific books: “Near Threshold Computing”, Springer (2015), “Low-Power Networks-on-Chip”, Springer (2010) and “Multi-objective design space exploration of multiprocessor SoC architectures”, Springer (2011); Co-author of the scientific book: “Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems”, Kluwer Academic Publisher (2003);
- Inventor/Co-inventor of **11 patent applications** with Group Bull or STM (**7 out of 11 already granted**).

Based on [Google Scholar](#) (21/11/2016), my h-index is **29**, my i10-index is **70** and my total number of citations is **2833**.

SCIENTIFIC SERVICES

I am an active contributor to the scientific community and I regularly serve as **Member** (or **Track Chair**) of the Program Committee of several top-level conferences such as **DAC**, **ICCAD**, **DATE**, **NOCS**, **HPCA**, **MICRO**, **ASAP** and **FPL**. Recently I was **Program Chair of FPL 2015**, the 25th International Conference on Field Programmable Logic and Applications. Previously I was **Program Co-Chair of ASAP2012**, **ARC2011**, and **SASP2010**. I was **General Co-Chair of SASP2009** and **MICRO2008** (receiving the ACM Recognition of Service Award). I have also organized several international workshops as **Program** or **General Chair**. From June 2015, I am **Associate Editor** of ACM Transactions on Architecture and Code optimization (TACO). I have served as **Independent Expert Reviewer** for the European Commission and for several science foundations such as the **Agence National de la Recherche** (F), the **Swiss National Science Foundation** (CH) and the **Academy of Finland**. I have been invited to give several talks/seminars and moderate panels all over the world.

ACADEMIC SERVICES

I balanced my effort in teaching at Undergraduate and M.Sc. levels. I annually teach basic courses on **Computer Architectures** and **Operating Systems** and M.Sc. courses on **Advanced Computer Architectures**. I enjoy teaching and I have an extensive English-speaking teaching experience started at Como Campus of POLIMI in 2004. I am an active contributor to the organisation of teaching activities in Computer Engineering at POLIMI, mainly at Como Campus, where I am Chairing the Committee on Undergraduate Study Plans and Student Transfers. I am also Member of the Committee on Graduate Admissions at POLIMI. I was advisor of **60+ M.Sc. students** and advisor/co-advisor of **12 Ph.D. students**.

INDUSTRIAL EXPERIENCE

I started my career as **Design Engineer** and then become **Senior Design Engineer** at the **R&D Labs of Group Bull** in Italy (1987-1996). Since 1992, I was part of the **Bull-IBM Research** team for the design of the first worldwide multiprocessor system based on **PowerPC** architecture. These multiprocessors have been commercialized as **Bull Escala** UNIX Servers and as **IBM RS/6000** Multiprocessor Servers. I also spent several periods abroad as **Visiting Engineer** at Bull R&D Labs, Billerica (MA - USA), **Visiting Engineer** at VLSI Technology, in Munich (D) and in S. Jose (CA-USA) and **Visiting Engineer** at IBM Somerset Design Center, Austin (TX - USA).

CURRICULUM VITAE - CRISTINA SILVANO

INDEX

1.	PERSONAL DATA AND CAREER.....	3
1.1.	EDUCATION	3
1.2.	ACADEMIC CAREER.....	3
1.3.	INDUSTRIAL CAREER	4
2.	RESEARCH ACTIVITIES	5
2.1.	RESEARCH TOPICS AND MAIN ACHIEVEMENTS	5
2.2.	RESEARCH COLLABORATIONS.....	9
2.3.	COORDINATION OF EUROPEAN RESEARCH PROJECTS	10
2.4.	COORDINATION OF INDUSTRIAL FUNDED RESEARCH PROJECTS	11
2.5.	PARTICIPATION TO EUROPEAN RESEARCH PROJECTS.....	11
2.6.	PARTICIPATION TO NATIONAL RESEARCH PROJECTS	11
2.7.	PARTICIPATION TO INDUSTRIAL FUNDED RESEARCH PROJECTS	12
2.8.	EVALUATION OF RESEARCH PROJECTS FOR THE EUROPEAN COMMISSION:	12
2.9.	EVALUATION OF RESEARCH PROJECTS FOR VARIOUS SCIENCE FOUNDATIONS	12
3.	SCIENTIFIC SERVICES.....	13
3.1.	ORGANIZING COMMITTEE MEMBER	13
3.2.	PROGRAM COMMITTEE MEMBER.....	14
3.3.	ASSOCIATE/GUEST EDITOR AND JOURNAL REVIEWER	15
3.4.	INVITED TALKS, SEMINARS AND PANELS.....	15
3.5.	MEMBER OF PROFESSIONAL ORGANIZATIONS	17
4.	ACADEMIC SERVICES	18
4.1.	TEACHING ACTIVITIES AT UNIVERSITIES.....	18
4.2.	ACADEMIC RESPONSIBILITIES	20
4.3.	RESEARCH ADVISING.....	21
4.4.	PHD EXTERNAL EXAMINER.....	21
4.5.	VISITORS	22
5.	LIST OF PATENTS AND AWARDS	23
5.1.	PATENTS	23
5.2.	AWARDS	23
6.	LIST OF PUBLICATIONS	24
6.1.	INTERNATIONAL JOURNALS WITH PEER REVIEW	24
6.2.	INTERNATIONAL BOOKS.....	25
6.3.	EDITORIAL CONTRIBUTIONS.....	26
6.4.	CHAPTERS IN INTERNATIONAL BOOKS WITH PEER REVIEW	27
6.5.	ACADEMIC TEXTBOOKS (IN ITALIAN)	28
6.6.	INTERNATIONAL CONFERENCES AND WORKSHOPS WITH PEER REVIEW	28
6.7.	INVITED PAPERS AND WORKSHOPS WITH INFORMAL PROCEEDINGS	34

1. PERSONAL DATA AND CAREER



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Born in Milan (Italy), December the 25th, 1961. Living in Milan (Italy).

Languages: Italian (mother tongue); English (fluent); French (good reading and listening); Spanish (basics).

My career is twofold. In 1987, after graduation at Politecnico di Milano, I have started my **industrial career** as Design Engineer (then upgraded as Senior Design Engineer) at the R&D Labs of Group Bull (Italy) spending several periods abroad as Visiting Engineer. Almost a decade later, to follow my interests in the scientific research and my attitude towards teaching, I have started my **academic career** as Ph.D. student at Università degli Studi di Brescia (Italy). After my Ph. D., received in 1999, I have continued as Post-Doc Researcher at CEFRIEL and at Politecnico di Milano, Assistant Professor at Università degli Studi di Milano (2000-2002) and Associate Professor at Politecnico di Milano (2002-present).

1.1. EDUCATION

- **Dottorato di Ricerca in Ingegneria dell'Informazione (Ph.D. in Computer Engineering)**, Università degli Studi di Brescia (Italy), 1999. Ph.D. Thesis on: "Power Estimation and Optimization Methodologies for Digital Circuits and Systems", Advisor: Prof. P. Gubian, Università degli Studi di Brescia, Co-Advisor: Prof. D. Sciuto, Politecnico di Milano.
- **Laurea in Ingegneria Elettronica (Master of Science in Electrical Engineering)**, Politecnico di Milano, 1987 (Final grade 100/100). MS Thesis on: "Theoretical and numerical study of shallow waters fluid dynamic models", Advisor: Prof. G. Prouse, Politecnico di Milano, Co-Advisor: Prof. L. Gotusso, Politecnico di Milano.

1.2. ACADEMIC CAREER

- I have recently named **IEEE Fellow** (effective from 2017) by the IEEE Boards of Directors "for contributions to energy-efficient computer architectures".
- In December 2013, I have received the Scientific National Qualification in Italy as **Full Professor** in sector 09/H1 Information Processing Systems and in sector 01/B1 Informatics (as defined in DD222 of July 20, 2012).
- **Associate Professor** (from 01/09/2002; with **tenure** from 01/09/2005) in Computer Engineering at Politecnico di Milano, Department of Electronics, Computer Engineering and Bioengineering (DEIB). I annually teach basic and advanced courses on Computer Architectures and Operating Systems. My primary research interests are in the areas of Computer Architecture and Electronic Design Automation, with particular emphasis on power-aware design, design space exploration for embedded architectures, adaptive design and monitoring of applications for many-core architectures, many-core architectures based on Networks-on-Chip, technology-aware many-core architectures and fault tolerant coding techniques.
- **Assistant Professor** (01/10/2000 - 31/08/2002) in Computer Science at Università degli Studi di Milano, Department of Computer Science. I was annually teaching basic and advanced courses on Computer Architectures and Operating Systems. My research activity was mainly focused on power-aware computing for embedder processor architectures.
- **Post-Doc Researcher** (Assegnista di Ricerca) (01/9/1999 - 30/09/2000) at Politecnico di Milano, Dipartimento di Elettronica e Informazione. Main research topic: "Computing Architectures: testing and simulation systems" (Supervisor Prof. D. Sciuto, Politecnico di Milano). My research activities were also related to the research project on "Power estimation methodologies for VLIW architectures", in collaboration with STMicroelectronics.
- **Post-Doc Researcher** (01/01/1999 - 31/08/1999) at CEFRIEL (Center for the Research and the Education in Information Engineering, Milan), Electronic Design Automation Area. My research activity was mainly part of the research project TOSCA (Tools for System Co-design Automation) and the European Project No. 26796 PEOPLE (Power Estimation for fast exPLoration of Embedded systems) under the supervision of Prof. D. Sciuto.
- **Ph.D. Student** (01/03/1996 – 31/12/1998) at Università degli Studi di Brescia (Italy), Dipartimento di Elettronica per l'Automazione. My research activity was mainly focused on power estimation and optimization methodologies for embedded architectures. Ph.D. defense held in 1999.

1.3. INDUSTRIAL CAREER

From May 1987 to February 1996, I was employee at the **R&D Laboratories of Groupe Bull** (also known as Bull HN Information Systems), Pregnana Milanese (Italy) where I held the position of **Design Engineer** up to March 1993 and **Senior Design Engineer** up to February 1996. During my experience at Groupe Bull, I have been involved in the following research and development activities:

- From September 1988 to October 1990, I was part of the design team of a full-custom 32-bit Central Processing Unit including a virtual memory management unit. The CPU was designed for a system based on the GCOS6 Bull proprietary OS. During the design, I was **Visiting Engineer** at the **Bull R&D Labs, Billerica (MA - USA)** in Fall 1988 and in Spring 1989. I also was **Visiting Engineer** at the VLSI design center of **VLSI Technology Inc., Munich (Germany)** from February-March 1990, and at **VLSI Technology Inc. in S. Jose (CA-USA)** in April 1990. For my contribution to the microprocessor design and verification, I received the **"1991 Bull Technical Award"**.
- In 1990, I designed a Dual Port SRAM module generator based on a process-independent design methodology. The generator has been used to synthesize two embedded memories integrated in a VLSI circuit designed for the European project ESPRIT2 -IDPS (Integrated Design and Production System) No. 5075 (1990-1992). In 1992, I have applied as co-inventor of a hierarchical and modular memory architecture in one **European patent** [P1-EU] granted in 1997.
- From 1991 to July 1992, I was with the Bull Advanced Technology Group, responsible for the introduction of new technologies and methodologies in the design of integrated circuits for Bull computer systems.
- Since August 1992, I was part of the **Bull-IBM Research (Austin-US)** design team of the chip set for the Bull Escala multiprocessors, which are symmetric and scalable systems based on shared memory architecture and composed of two to eight processors. The Escala systems have been **the first worldwide multiprocessors based on the PowerPC architecture** (introduced in 1992 by the Apple-IBM-Motorola alliance, then generating the PowerPC 601, 604e e 620 processors). The first implementation of the architecture was the PowerPC 601 released by IBM in 1992. The Escala systems have been fully developed by a Bull-IBM joint team at the R&D Bull Labs and then commercialized as **Bull Escala UNIX Servers** and **IBM RS/6000 Symmetric Multiprocessor Servers** (named also as **RS/6000 POWERserver** servers, **RS/6000 POWERstation** and then renamed as **eServer pSeries** in October 2000). During the Bull-IBM joint project, I also was **Visiting Engineer** at **IBM Somerset Design Center, Austin (TX - USA)** in Fall 1993 and in Spring 1994. For the research and development of the Escala/RS6000 multiprocessor systems, my main contributions were:
 - From August 1992 to May 1993, I was in the design team of the chip-set implementing the 64-bit data cross bar architecture, named **PowerScale**, connecting four processor nodes (including two processors each), the I/O node (including two I/O channels), and the shared memory. The PowerScale architecture has been adopted by many commercial series of the Bull Escala servers. The chip-set includes a new error detection and correction code to improve system reliability and data integrity. From this code, I developed the construction techniques for a new class of codes for computer memory sub-systems. For the new class of codes, I applied as Inventor in one **European Patent (granted in 1998)** [P2-EU] and in one **US Patent (granted in 1996)** [P2-US].
 - From June 1993 to July 1994, I was in the design team of a 120K gates VLSI circuit with the functionality of Secondary Cache Controller for both PowerPC 601 and 604 processors. The circuit implements the cache coherency mechanism both vertically (between the different cache levels of each processor) and horizontally (among different processors). The cache coherency is based on the MESI protocol.
 - From September 1994 to December 1995, I was in the team for the design and simulation of a 230K gates VLSI circuit with the functionality of Memory Controller, based on a shared and interleaved memory sub-system. The circuit manages also the data-cross bar architecture, PowerScale, for the new series of multiprocessor systems: Escala-E and Escala-T. More in detail, The Escala-E servers support up to two processors (PowerPC 604e or 620), the shared memory configurable from 16MB to 2 GB, and a single 64-bit PCI bus. The Escala-T servers support up to four processors (PowerPC 604e or 620), the shared memory configurable from 32 MB to 3 GB, and two 64-bit PCI buses.
- During the Academic Years 1993/94 and 1994/95, I also held the position of **Bull Senior Researcher**, supervisor of some Master students in Information Technology at **CEFRIEL – Research and Training Center** in Milano in the Electronic Design Automation area. The activities were partially funded by the European Project EUREKA/JESSI (Joint European Submicron Initiative) – Subprogram Application AC-5.

2. RESEARCH ACTIVITIES

2.1. RESEARCH TOPICS AND MAIN ACHIEVEMENTS

My research is primarily focused on the areas of **Computer Architectures** and **Electronic Design Automation**, with particular emphasis on the following research topics (*listed hereafter in chronological order*). For each research topic, the most significant achievements are also reported.

2.1.1. Fault Detection and Fault Tolerant Coding Techniques

The research faced with Error Control Coding techniques to improve the fault detection and fault tolerance in computing systems. Main goals of the research were, from one side, the design of a new class of error detection and correction codes and, from the other side, the definition of detection codes for unidirectional errors. Starting from the proposed coding schemes, a set of automatic tools to support the design of the proposed coding techniques has been defined.

Main achievements: My contribution to the field was the introduction of a new class of systematic SEC-DED (Single Error Correction – Double Error Detection) codes with single byte error detection capability published in **IEEE Trans. on Information Theory 1995** [J28]. An automatic code generation framework was developed and published in **IEEE Trans. on VLSI 1998** [J25]. For the new class of codes, I have been designated as **inventor** in both the **European Patents** [P2-EU] granted in 1998 and in the **US Patent** [P2-US] granted in 1996. An implementation of the new class of error detection and correction codes has been part of the PowerScale architecture commercially adopted by the **Bull Escala** and **IBM RS6000** multiprocessor systems.

2.1.2. Power-Aware Computing for Embedded Architectures

Power dissipation has been identified as the main performance limiter for high-performance processors, while power dissipation limits the capabilities of battery-powered embedded mobile devices and wireless sensor nodes. My research on power-aware design started in 1996, at the beginning of my Ph.D. program (under the supervision of my co-advisors, prof. P. Gubian and prof. D. Sciuto). The main goal of my Ph. D. research was to develop design techniques for the analysis and synthesis of digital circuits and systems to reduce the power consumption at the higher levels of abstraction. The research activity was mainly focused on the estimation and optimization of power dissipation. Then I started my Post-Doc at Politecnico di Milano (under the supervision of my mentors, prof. D. Sciuto and prof. M. Sami) and my research moved towards the investigation of power-aware techniques for embedded architectures based on VLIW (Very Long Instruction Word) pipelined processors. My post-doc research on low-power VLIW architecture has been carried out in collaboration with Vittorio Zaccaria (at that time Ph.D. student at Politecnico di Milano). The proposed techniques have been applied to the **Lx/ST200** family of VLIW embedded processor cores (developed as a partnership between HP Labs and STMicroelectronics). The ST200 family (including the ST210, ST220, ST231 processor cores) was widely used for embedded media processing in a variety of audio, video and imaging consumer products.

Main achievements: The most significant achievements of my Ph.D. thesis on high-level power estimation have been published in **IEEE Trans. on VLSI-1998** [J26] and **JSA-1997** [J27]. My Ph.D. thesis research represents one of the first efforts to face the problem of power-aware bus encoding for processor-to-memory communication by exploiting spatial-temporal locality. Main achievements of my Ph.D. thesis related to low-power bus encoding techniques have been published in **GLS-VLSI-1997** [C85] and **DATE-1998** [C82]. These two early papers in my career have had a high research impact: so far, they have had **336** and **164** citations respectively, still representing *my top ranked papers*. The paper presented at **DATE-1998** [C82] has also been selected in 2008 as a chapter of the volume: *“The Most Influential Papers of 10 Years DATE”* [CH12]. For the design of a low-power encoder/decoder architecture (developed in collaboration with STMicroelectronics), I have been designated as co-inventor in the **European Patent Application** [P3-EU] published in 2001 and in the **US Patent Application** [P3-US] published in 2002.

The most significant achievements of my Post-Doc research were: *(i)* to develop the first and most comprehensive power estimation framework at the instruction-level validated on an industrial VLIW architecture (the Lx/ST200 family), *(ii)* the definition of an innovative register file write inhibition scheme to exploit forwarding paths in the pipeline to save power when accessing short-lived variables; *(iii)* the definition of power-aware branch prediction techniques based on compiler hints for VLIW processors. More in detail, the instruction-level energy model for VLIW pipelined processors has been published in **CODES-2000** [C73], **ICCAD-2000** [C71] and then extended to the **IEEE Trans. on CAD-2002** [J23]. Results on the reduction of the complexity of the energy model by introducing the concept of instruction clustering have been presented in **DAC-2002** [C65], then extended in **DAES-2005** [J19] and **PATMOS-2001** [C67]. Results on power optimization of the pipeline forwarding paths and branch prediction for VLIW have been published in **DATE-2001** [C70], **GLS-VLSI-2003** [C61], **GLS-VLSI-2004** [C58] then extended to **IEEE Trans. on VLSI-2002** [J21] and **Integration-2005** [J20]. For the low-power forwarding architecture, I have been designated as co-inventor in the **US Patent** [P4-US] granted in 2005. Finally, most significant contributions on power-aware VLIW design techniques have been collected in 2003 in the **scientific book**: *“Power Estimation and*

Optimization Methodologies for VLIW-based Embedded Systems" [B4] published by Kluwer Academic Publishers.

The research experience and accomplishments on power-aware computing lead me towards one of my primary **on-going** research paths: design space exploration techniques for computing architectures from a combined power/ performance perspective.

2.1.3. **Design Space Exploration of Embedded Architectures**

Given the complexity of multi/many core architectures, system optimization and exploration definitely represent challenging research tasks. A wide range of design parameters must be tuned from a multi-objective perspective, mainly in terms of performance and energy consumption, to find the most suitable system configuration for the target application. Multi-objective exploration of the huge design space of multi/many core architectures definitely needs for automatic **Design Space Exploration (DSE)** techniques to systematically explore the design choices and to compare them in terms of multiple competing objectives (trade-offs analysis). The aim of my research (carried out mainly in collaboration with Vittorio Zaccaria and Gianluca Palermo at POLIMI) was to investigate on power/performance trade-offs in application-specific embedded architectures. The exploration techniques are based on multi-objective optimization algorithms and energy/delay estimation metrics. The main goal is to provide an automatic DSE methodology and tool for the analysis of system characteristics and the selection of the most appropriate architectural solution to satisfy power/performance system requirements. A set of heuristic optimization algorithms have been defined to prune the design space to be explored, while a set of response surface modeling techniques have been defined to further speed up the exploration time. The basic idea was defining an analytical response model of the system behavior based on a subset of system simulations to predict the unknown system response. The proposed DSE framework (namely MULTICUBE Explorer) leverages a set of open-source tools for the exploration, modeling and simulation to guarantee a wide exploitation of the project results in the embedded system design community. Research on DSE techniques have mainly been carried out in the context of the **FP7-MULTICUBE** European project under my scientific coordination.

Main achievements: The primary contribution of my research was to define an automatic multi-objective DSE methodology and related framework (MULTICUBE Explorer) to tune embedded on-chip platforms finding the best power/performance trade-offs, while meeting system-level constraints and speeding up the exploration process. Under the premises of the MULTICUBE project, MULTICUBE Explorer open-source tool has been developed and validated on STMicroelectronics and IMEC virtual platforms. Benefits of the MULTICUBE design methodology and tools have been assessed on a number of industrial use cases provided by STMicroelectronics and IMEC.

The most significant results of my research on DSE have been published in top-ranked journals like **DAES-2002** [J24], **DAES-2007** [J15], **IEEE Trans. on CAD 2009** [J11], **IEEE Trans. on CAD 2012** [J9], and in several conferences: **CODES-2001** [C69], **DATE-2003** [C64], **SAC-2003** [C63], **GLS-VLSI-2003** [C62], **PATMOS-2003** [C60], **SAC-2004** [C59], **SASP-2008** [C44], **SAMOS-2008** [C43], **SAMOS-2009** [C34], **SASP-2009** [C33], **DAC-2010** [C27] and **SASP-2011** [C25]. I was also **Co-editor** of the scientific book: "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Springer, 2011 [B3].

More recently, my research work on DSE has been evolved to: (i) the exploration based on predicting simulation scheduling published at **DATE-2014** [C11] and extended in **IEEE Transactions on CAD 2015** [J2]; (ii) optimising the high-level synthesis process published at **DATE-2013** [C16] and extended in **IEEE Transactions on CAD 2015** [J3].

2.1.4. **Adaptive Design and Monitoring of Applications for Many-core Architectures**

Based on the knowledge on *design-time* multi-objective exploration, my research path evolved towards the definition of a *runtime* methodology to optimize the allocation and scheduling of different application tasks on the underlying resources of the target many-core architecture. In 2007, to address this problem, a two-step approach has been devised in collaboration with IMEC researchers and Giovanni Mariani (at that time, Ph.D. student at University of Lugano, CH). First, the design exploration flow generates a Pareto-optimal set of design alternatives in terms of power/performance trade-offs. Second, this set of operating points can be used at *runtime* to decide how system resources should be allocated to different tasks running on the many-core system. Research on runtime resource management techniques have mainly been carried out in the context of the **FP7-2PARMA** European project under my scientific coordination. During 2PARMA project, the proposed runtime methodology has been applied to several application domains to demonstrate their applicability and benefits in industrial contexts, such as the P2012/STHORM many-core platform provided by STMicroelectronics. In this context, the research work of Edoardo Paone (Ph.D. student at Politecnico di Milano) was focused on the customisation and optimisation of OpenCL applications for the efficient task mapping under heterogeneous platform constraints. Relevant results in collaboration with Edoardo Paone have been published in **CODES-ISSS-2012** [C19], **DATE-2013** [C17], and **DATE-2015** [C4],

I believe dynamic runtime systems still provide many opportunities for energy savings. Some new research paths have recently been opened. Research is **on-going** on approximate and adaptive computing for power-aware embedded systems. Since optimizing computing systems for all worst case scenarios is not a feasible approach, we have to start thinking at systems that are capable to **self-adapt** dynamically to changing operating conditions

and environments. The lack of autotuning and runtime adaptation capabilities at the application level tends to lead to sub-optimal power/performance trade-offs at the system level due to the underutilisation of the resources in a many-core architecture. The proposed approach borrows some concepts derived from the approximate and adaptive computing area to give to the application some **autotuning** capabilities. The system-wide adaptive approach is based on global monitoring, adaptation and optimization. Appropriate self-adaptive techniques are provided to dynamically support migration of code and data among cores. In the context of **heterogeneous** many-core architectures, we can devise support for code and data migration between different types of processing cores, thus capable to adapt to several processor architectures and hardware accelerators. Joint research with the **Technical University of Delft (NL)** was focused on runtime optimization techniques of dynamically reconfigurable systems. The most relevant results have been published in **FPL-2013** [C15] and **ASP-DAC-2014** [C12]. I believe there are still significant paths dealing with heterogeneity in the era of many-cores based on accelerator-centric architectures and dynamic task mapping.

The research experience gained on adaptive computing for heterogeneous many-cores lead me towards one of my recently-opened research paths: The application autotuning combined with the runtime power management of **High Performance Computing** systems. This research path represents the core concept I have proposed as Scientific Coordinator in the **H2020 ANTAREX** research project, accepted for funding under the FET-HPC European initiative in 2015. The main goal of the project is to provide a breakthrough approach to express by a Domain Specific Language the application self-adaptivity and to runtime manage and autotune applications for green and heterogeneous HPC systems. I believe the ANTAREX project represents a very promising and challenging research path up to the Exascale era, expected to be reached in 2023.

Main achievements: The main contribution of my research was on the exploitation of the synergy of *design-time* and *runtime* techniques to get an effective approach towards a power-aware adaptive computing. The main outcomes of the research on adaptivity and runtime management techniques have been published in **DATE-2010** [C28], **IET-2011** [J10], **DATE-2012** [C21] and more recently in **ARC-2014** [C9], **ASAP-2014** [C8], **IC-SAMOS-2014** [C7], **ISPA-2014** [C6], **DATE-2015** [C4], **IC-SAMOS-2015** [C3]. Some of the main achievements have been published in the journal papers **PARCO-2013** [J6] and **ACM Trans. on Embedded Computing Systems 2013** [J5].

More recently, I have presented the seminal research concepts of the ANTAREX project at **EUC-2015** [IP2], **CF-2016** [IP1] and **DATE-2016** [C2]. In the context of ANTAREX, my research has recently been focused on compiler autotuning based on machine learning techniques in collaboration with Amir H. Ashouri, currently Ph. D. student at POLIMI. The most significant results have been published in **TACO-2016** [J1].

2.1.5. *Many-core Architectures based on Networks-on-Chip*

Given the increasing complexity of many-core architectures, the current trends on on-chip communication are converging towards the Network-on-Chip (NoC) approach, representing a high bandwidth and low energy solution. Using the NoC-based design approach has several other advantages, such as scalability, reliability, IP reusability and separation of IP design from on-chip communication design and interfacing. NoC design represents a new paradigm to design multi/many-cores shifting the design methodologies from computation-based to communication-based. To address these NoC research challenges, a new path of my research started in 2003 focusing on the topic of low-power NoC for embedded architectures, covering energy aware design and techniques from several perspectives and abstraction levels. My research on NoC started as advisor of Gianluca Palermo (at that time Ph.D. student at Politecnico di Milano) focusing on the development of **PIRATE**, a modular and flexible framework for power/performance exploration of Network-on-Chip architectures. The PIRATE framework has then been applied to explore distributed shared memory architectures based on NoC. For this class of systems, I have also started a new research path to investigate the problem of synchronization mechanisms and memory management techniques. Most of my research on low-power NoC for embedded architectures have been carried out in the context of two industrial research projects funded by **STMicroelectronics**. I was **Principal investigator** in both research contracts, namely: "*Low Power Network on Chip and Embedded Architectures*" (2003-2005) and "*Low Power Network on Chip and Multiprocessor Platforms*" (2006-2008).

Then my research was addressing the problem of the application mapping, optimization and topology customization for the **Spidergon NoC** architecture provided by STMicroelectronics (Grenoble, F). My research on **ST Spidergon NoC** has been carried out in the context of the **MEDEA+ LoMoSA+** project.

In that period, I have started working with prof. D. Sciuto co-advising the Ph.D. thesis of Giovanni Beltrame on modeling, simulation, analysis and optimization of Multi-Processor System-on-Chip platforms. My contribution was mainly to support the Network-on-Chip modeling and exploration. The target platform has been configured to simulate an IPv4 forwarder (based on the StepNP framework developed at STMicroelectronics Research Labs, Ottawa), an MPEG4 VGA encoder, and an Ogg-Vorbis encoder. These applications have been modeled by introducing a multi-accuracy transaction-level approach, then explored and optimized in terms of power and performance.

In 2007, I have started investigating about security aspects in NoCs together with Gianluca Palermo and Leandro Fiorin (Ph.D. student at University of Lugano, CH). Our seminal work appeared at **CODES-ISSS 2007** [C47] still remains to this day one of the first approaches to investigate an important but unaddressed aspects of NoCs, namely *security*. The work has then been extended in **IEEE Trans. on Computers 2008** [J12]. Afterwards, we opened a new research path by adding high level services on top of the standard communication services usually provided by an interconnection network. Research on run-time monitoring through NoC are still ongoing under my scientific coordination in collaboration with **ALaRI Research Institute** based at the University of Lugano (CH). Moreover, on-going joint research with the **Universidade Federal do Rio Grande do Sul** in Porto Alegre (Brasil) is focused on floor planning-aware exploration for application-specific NoC and adaptive buffers for virtual channel routers in NoCs.

Main achievements: Main research achievement of my early research on NoC were: (i) the development of **PIRATE** framework for NoC optimization (presented in **PATMOS-2004** [C57]) and (ii) the development of **GRAPES** modeling and simulation framework for multi-processor Systems-on-Chip based on NoC presented at **IC-SAMOS-2006** [C53] and then extended in **JSA-2007** [J14]. One of the most significant results of the research team I was leading at that time at Politecnico di Milano (and composed of Matteo Monchiero, Gianluca Palermo and Oreste Villa) was the definition of optimized **synchronization techniques** for distributed shared memory multi-core architectures based on Network-on-Chip. The proposed synchronization techniques appeared in high-impact venues: **DATE-2006** [C54], **ACM SIGARCH-2006** [J17], **IEEE Transactions on VLSI 2006** [J16] and then **CASES-2008** [C59].

The main outcomes of the research done in collaboration with prof. Donatella Sciuto and Giovanni Beltrame have been published in the Proceedings of top-level conferences (**CASES-2004** [C56], **DATE-2006** [C55] and **CODES-ISSS-06** [C51]) then extended in the **IEEE Trans. on CAD 2007** [J13].

Concerning our pioneer work on NoC security, the most relevant research result is represented by a data protection unit for NoC architectures presented first at **CODES-ISSS-2007** [C47], then extended in the prestigious **IEEE Trans. on Computers 2008** [J12]. Our work on the programmable data protection device and secure programming manager has been the subject of **one European patent** application [P5-EU] in collaboration with STMicroelectronics, afterwards extended to **one US Patent granted in 2012** [P5-US].

Afterwards, secure monitoring services for NoCs have been presented in **CODES-ISSS-2008** [C37], while a run-time monitoring system based on NoCs has been proposed in **DATE-2009** [C35] and recently extended in the **IEEE Trans. on VLSI-2013** [J4]. Finally, I was also **Co-editor** of the scientific book: "Low-Power Networks-on-Chip" published by Springer in 2011 [B2].

2.1.6. **Technology-aware Many-core Architectures Design**

A basic tenet of my research is that power-aware application-specific many-core architectures must be tuned being aware of microarchitectural and technology problems and emphasizing the early-phase of design space exploration. Many challenging and relevant research topics related to many-core architectures are still open. There is still significant research to be done, and architectural and technology challenges will increase in importance as we scale down the fabrication process in the nanoscale era. I believe that technology-driven considerations (such as ultra-low-power design, resiliency and process variability) will further increase their importance on architecture and system level design in the next coming years. In the many-core era, system design optimization and exploration still represent challenging tasks. Networks-on-Chip, as an architectural solution for scalable high speed interconnect, and power-aware design will continue to be crucial topics, since power and energy issues still represent one of the limiting factors in integrating multi/many cores on a single chip. The power-wall problem and its dual utilization-wall problem are considered among the main barriers for an efficient performance scaling bringing to the **dark silicon** problem (where for dark silicon is intended the chip fraction not usable in a many-core chip due to the power budget). To address the dark silicon problem, **Near Threshold Computing (NTC)** has recently been proposed as a promising solution to mitigate the dark silicon effects by operating at lower frequency but exploiting a larger number of cores. However, NTC suffers from an increase sensitivity to technology problems (such as process variability).

In this context, I have recently opened a new research path in collaboration with Gianluca Palermo and Sotirios Xydis (currently Post-doc at the National Technical University of Athens, formerly Post-doc at POLIMI) and Ioannis Stamelakos (currently Ph.D. student at POLIMI). The main focus of our research is on **variability-aware NTC** architectures based on the formation of voltage islands with emphasis on voltage and workload allocation across the many-core architecture. We also introduced the usage of approximate computing concepts to sustain performance despite of variability effects.

Main achievements: Our former research works on variability-aware robust DSE for many-core architectures have been published in **ASP-DAC-2009** [C36] and in **ACM Trans. on Embedded Computing Systems 2012** [J8]. Our most recent achievement consists of a variability-aware framework based on fine-grained voltage islands for exploring the potential power-efficiency of NTC under performance constraints. The proposed approach has been

presented in high-impact venues: **ASP-DAC 2014** [C13], **DATE 2014** [C10] and more recently in **ISVLSI-2016** [C1]. Finally, I was also **Co-editor** of the scientific book “**Near Threshold Computing**” published by Springer, 2015 [B1].

2.2. RESEARCH COLLABORATIONS

My research activities have been done in collaboration with several national and international universities, research centers and several ICT and semiconductor companies. Among them, we can mention:

1. **ALaRI** - Advanced Learning and Research Institute - Switzerland (2003 - Present), Contact Person: prof. M. Sami. Research topics: Design space exploration techniques based on response surface methods. Design and analysis of high-level services for Network on-Chip architectures.
2. **IMEC** - Interuniversity Micro-Electronics Centre, Belgium (2007 - Present), Contact Persons: prof. Francky Catthor, Chantal Ykman Couvreur, Research topic: Design and analysis of an application-specific manager for power-aware adaptation.
3. **STMMicroelectronics** - Agrate, Italy (1996 - Present), Contact Person: Dr. R. Zafalon. Research topics: Power estimation and optimization techniques for Network on-Chip architectures (1996 – 2006); Design space exploration of embedded computing architectures (2007 – Present).
4. **STMMicroelectronics** - Grenoble, France (2005 - 2007), Contact Person: Dr. M. Coppola. Research topic: Design methodology and implementation of high-level services on the ST-NOC architecture.
5. **STMMicroelectronics** - Grenoble, France (2010 - 2013), Contact Person: Dr. D. Melpignano. Research topic: Design methodology and tools for many-cores computing fabrics.
6. **Fraunhofer - Heinrich Hertz Institut** – Berlin, Germany (2010 – 2013), Contact Person: Dr. Benno Stabernack. Research topics: Design space exploration of Scalable Video Coding applications
7. **NTUA** - National Technical University of Athens - Greece (2010 - Present), Contact Persons: prof. D. Soudris, Dr. S. Xydis. Research topics: Runtime management techniques for many-core architectures; Design and exploration of Near-Threshold Computing architectures.
8. **TU Delft** – Technical University Delft, The Netherlands (2008 - Present), Contact Person: prof. K. Bertels. Research topics: Design space exploration and run-time management techniques for reconfigurable computing platforms.
9. **PNNL** - Pacific Northwestern National Laboratory - WA, USA (2010 - Present), Contact Persons: Dr. A. Tumeo, Dr. O. Villa (currently at NVIDIA). Research topics: Design and analysis of a many-core/many-node architecture for irregular applications.
10. **UFRGS** - Universidade Federal do Rio Grande do Sul - Brazil (2009-Present), Contact Person: prof. L. Carro. Research topic: Floorplan-aware design methodology for Network on-Chip architectures.
11. **IBM Research** - ASTRON & IBM Center for Exascale Technology, The Netherlands (2013 – Present), Contact Persons: Dr. L. Fiorin and Dr. G. Mariani. Research topic: Architectures and applications for exascale computing.
12. **UCI** - University of California at Irvine – CA, USA (2013 – Present) Contact Person: prof. Fadi Kurdahi. Research Topic: Near Threshold Computing for many-core architectures.
13. **University of Delaware, USA (2014 – Present)**, Contact Person: prof. John Cavazos. Research Topic: Machine learning techniques for compiler optimization.
14. **CINECA, Italy (2015 – Present)**, Contact Person: Dr. Carlo Cavazzoni and Dr. Nico Sanna. Research Topic: Energy-efficient High Performance Computing systems.
15. **Universidade do Porto, Portugal (2015 – Present)**, Contact Person: Prof. Joao Cardoso. Research Topic: Application autotuning based on Domain Specific Languages
16. **ETH Zurich, Switzerland (2015 – Present)**, Contact Person: Prof. Luca Benini. Research Topic: Resource-aware energy-efficient High Performance Computing systems.

Research Collaborators/Co-authors/Co-Editors (with other affiliations) (about 70):

Gerd Ascheid (Aachen University, Germany), Prabhat Avasare (IMEC, Belgium), Andrea Bartolini (ETHZ, Switzerland), Sanzio Bassini (CINECA, Italy), Alex Bartzas (EXUS, Greece), Andrea Beccari (Dompé, Italia), Luca Benini (ETHZ, Switzerland), Mladen Berekovic (TU Braunschweig, Germany), Koen Bertels (Delft Technical University, The Netherlands), Sara Bocchio (STMMicroelectronics, Italy), Umberto Bondi (University of Lugano, Switzerland), Jens Brandenburg (Fraunhofer HHI, Germany), João Cardoso, (University of Porto, Portugal), Luigi Carro (UFRGS, Brazil), Jeronimo Castrillon (Dresden Technical University, Germany), Franky Catthor (IMEC, Belgium), John Cavazos (University of Delaware, USA), Carlo Cavazzoni (CINECA, Italy), Peter Cheung (Imperial College London, UK), Radim Cmar (Sygic, Slovakia), Caroline Concatto (UERGS, Brazil), Marcello Coppola (STMMicroelectronics, France), Giovanni De Micheli (EPFL, Switzerland), Giuseppe Desoli (STMMicroelectronics, Italy), Giovanni Erbacci (CINECA, Italy), Dongrui Fan (ICT - Chinese Academy of Sciences, China), Leandro Fiorin (IBM-ASTRON, The Netherlands), Franco Fummi (University of Verona, Italy), Arpad Gellert (Sibiu University, Romania), Carlo Guardiani (STMMicroelectronics, Italy), Paolo Gubian (University of Brescia, Italy), Zhang Hao (ICT - Chinese

Academy of Sciences, China), Michael Huebner (Ruhr Universitaat Bochum, Germany), Carlos Kavka (ESTECO, Italy), Torsten Kempf (Cognex Corporation, Germany), Fadi Kurdahi (University of California at Irvine, USA), Marcello Lajolo (NEC Labs, USA), Rainer Leupers (Aachen University, Germany), Wayne Luk (Imperial College London, UK), Enrico Macii (Politecnico di Torino, Italy), Giovanni Mariani (IBM-ASTRON, The Netherlands), Marco Martinez (DS2, Spain), Jan Martinovic (IT4Innovations, Czech Republic), Debora Matos (UERGS, Brazil), Diego Melpignano (STMicroelectronics, Italy), Smail Niar (University of Valenciennes, France), Luca Onesti (ESTECO, Italy), Martin Palkovic (IT4Innovations, Czech Republic), Pierre Paulin (Synopsys, Canada), Hector Posadas (University of Cantabria, Spain), Erven Rohou (INRIA, France), Ingo Sander (KTH, Sweden), Nico Sanna (CINECA, Italy), Michael Schulte (AMD, USA), Vlad-Mihai Sima (Bluebee, The Netherlands), Katerina Slaninova (IT4Innovations, Czech Republic), Dimitrios Soudris (National Technical University of Athens, Greece), Benno Stabernack (Fraunhofer HHI, Germany), Giulio Urlini (STMicroelectronics, Italy), Geert Vanmeerbeeck (IMEC, Belgium), Eugenio Villar (University of Cantabria, Spain), Lucian Vintan (Sibiu University, Romania), Vit Vondrak (IT4Innovations, Czech Republic), Marise Wouters (IMEC, Belgium), Sotirios Xydis (National Technical University of Athens, Greece), Chantal Ykman-Couvreur (IMEC, Belgium), Roberto Zafalon (STMicroelectronics, Italy)

2.3. COORDINATION OF EUROPEAN RESEARCH PROJECTS

- **Project Coordinator of the H2020-FET-HPC European Project ANTAREX-671623** on "AutoTuning and Adaptivity approach for Energy efficient eXascale HPC systems" (Sep. 2015 - Aug. 2018). www.antarex-project.eu The project won a 3 M€ grant in the H2020 Future and Emerging Technologies programme on High Performance Computing in 2015. The project involves leading academic and industrial partners as well as CINECA, the Italian Tier-0 supercomputing centre and IT4i, the Czech Tier-1 supercomputing center. Being one of the nineteen research projects in the FET-HPC-2014 Call, ANTAREX brings the partners on the forefront of the European research in High Performance Computing. The main goal of the ANTAREX project is to provide a breakthrough approach to express by a Domain Specific Language the application self-adaptivity and to runtime manage and autotune applications for green and heterogeneous High Performance Computing systems up to the Exascale level. The Consortium also includes three top-ranked academic partners (ETH Zurich, University of Porto, INRIA). Industrial partners include one of the leading biopharmaceutical companies in Europe (Dompé) and the top European navigation software company (Sygic).
- **Project Coordinator of the European Project FP7-2PARMA-248716** on "PARallel PARadigms and Run-time MAnagement techniques for Many-core Architectures" (Jan. 2010 – Mar. 2013). <http://www.2parma-project.eu/> EC Contribution to the project: 2.7 M€ funding. The 2PARMA Consortium was composed of seven partners: Politecnico di Milano (Italy), STMicroelectronics (Italy and France), Heinrich Hertz Institute - Fraunhofer Institute for Telecommunications (Germany), IMEC (Belgium), ICCS - Institute of Communication and Computer Systems (Greece), RWTH Aachen University (Germany), Synopsys (Belgium). The 2PARMA project focused on the definition of a parallel programming models, run-time resource management policies and design space exploration methodologies for many-core architectures. Applicability and benefits of the proposed techniques and tools have been validated and assessed on a set of industrial applications and hardware platforms. The 2PARMA project ended in March 2013 receiving a final overall rating of **"excellent"** (*the highest a project can get*) by the European Commission demonstrating the fulfillment of its objectives and scientific/technical goals. Based on the opinion of the European expert reviewers: *"the project represents a success story and has made significant contributions to the state-of-the-art in the field"*. Also the expected impact was considered to be **excellent**. Finally, the European expert reviewers commended me as Project Coordinator: *"for the efficiency and professionalism shown during the whole project; for demonstrating high management skills and strong leadership abilities and for establishing an efficient and effective collaboration amongst all the project partners"*.
- **Project Coordinator of the European Project FP7-MULTICUBE-216693** on "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (Jan. 2008 - June 2010). <http://www.multicube.eu/> EC Contribution to the project: 2.1 M€ funding. The MULTICUBE Consortium was composed of nine partners: Politecnico di Milano (Italy), Design of Systems on Silicon – DS2 (Spain), STMicroelectronics (Italy), IMEC (Belgium), ESTECO (Italy), University of Lugano - ALaRI (Switzerland), University of Cantabria (Spain), STMicroelectronics Beijing (China), Institute of Computing Technology – Chinese Academy of Sciences (China). The MULTICUBE project finished in 2010 with an **excellent final overall rating** by the EC demonstrating to fully achieve its objectives and scientific/technical goals. The project has demonstrated: the benefits of using automated design exploration techniques (based on enhanced multi-objective optimization) on a number of industrial use cases; practical ways to trade off accuracy for speed through the use of multi-abstraction level simulation thus enabling exploration of larger design spaces; the feasibility of automated parameter tuning at run-time using exploration data collected at design-time. Based on the opinion of the European expert reviewers, as Project Coordinator I have demonstrated *"high leadership capabilities and led very professionally all the management activities"*. In the context of the MULTICUBE project, I was also leading a research group at Politecnico di Milano whose research focuses on design space exploration for multi-processor architectures working on an open-source tool (**MULTICUBE Explorer**) to enable an automatic and fast optimization of configurable system

architectures towards a set of objective functions such as energy and delay.

2.4. COORDINATION OF INDUSTRIAL FUNDED RESEARCH PROJECTS

- **Project Manager** of the **IBM/Politecnico di Milano Collaborative Innovation Center on Big Data Analytics** (2015-Present).
- **Principal Investigator (Responsabile Scientifico)** in the two-year research project: "Low Power Network on Chip and Multiprocessor Platforms" (2006-2008) between the Dipartimento di Elettronica e Informazione of Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics**, Agrate B.
- **Principal Investigator (Responsabile Scientifico)** in the two-year research project: "Low Power Network on Chip and Embedded Architectures" (2003-2005) between the Dipartimento di Elettronica e Informazione of Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics**, Agrate B.

2.5. PARTICIPATION TO EUROPEAN RESEARCH PROJECTS

- Participation to the **European Integrated Project CONTREX - 611146** on "Design of embedded mixed-criticality CONTROL systems under consideration of EXtra-functional properties" (Oct. 2013 – Sep. 2016). <https://contrex.offis.de/home/> EC Contribution to the project: 6 M€. The CONTREX project includes fourteen partners from six countries. Project Coordinator: OFFIS (D). Local Principal Investigator: prof. W. Fornaciari.
- Participation to the **European Project FP7-HARPA-612069** on "Harnessing Performance Variability" (Sep. 2013 – Aug. 2016). <http://www.harpa-project.eu/> EC Contribution to the project: 2.8 M€. The HARPA project includes eight partners from six countries. Project Coordinator: prof. W. Fornaciari, Politecnico di Milano.
- Participation to the **ARTEMIS-2009-1-100230 SMECY Project** on "Smart Multicore Embedded Systems" (Feb. 2010 – Jan. 2013). <http://www.smecy.eu> The SMECY project includes thirty partners (among them STMicroelectronics and Thales) from nine European countries for a total funding of 19 M€. Project Coordinator: Francois Pacull (CEA Leti, France). Local Principal Investigator: prof. D. Sciuto.
- Participation to the **European Integrated Project COMPLEX - 247999** on "Co-design and power management in platform-based design space exploration" (Dec. 2009 – Feb. 2013). <https://complex.offis.de/> EC Contribution to the project: 4.8 M€. The COMPLEX project included fourteen partners from six countries (including China). Project Coordinator: OFFIS (D). Local Principal Investigator: prof. W. Fornaciari.
- From 2006 to 2007, I collaborated as **Senior Researcher** with ALaRI-Advanced Learning and Research Institute, part of the Faculty of Informatics of the Università della Svizzera Italiana (USI) to the European research project **MEDEA+LoMoSA+ (2A708)**: "Low-power expertise for Mobile & multi-media System Applications". Project Coordinator: NXP Semiconductors (NL). Local Principal Investigator: prof. M. Sami. The activity carried out in this project has been the subject of one European **patent application** [P5-EU], afterwards extended to the USA (**US patent** [P5-US] granted in 2012).
- Participation to the **European Project MEDEA+(A207) Pocket Multimedia** "Silicon application platform for pocket multimedia" (2001 – 2004). Project Coordinator: ST Microelectronics. Local Principal Investigator: Roberto Zafalon. In 2005, the project has won the annual award for European collaborative innovation in Microelectronics, the "Jean-Pierre Noblanc Award for Excellence."
- Participation to the **European Project FP6 - ICODES – 004452** "Interface and communication based design of embedded systems" (2004-2007). Project coordinator: OFFIS (D). Local Principal Investigator: prof. D. Sciuto.
- Participation to the **European Project FP6 – PEOPLE - 26796** "Power EstimatiOn for fast exPLoration of Embedded systems" funded by ESPRIT4-OMI (Open Microprocessor Initiative) from 1/4/1998 to 31/12/2000. Project coordinator: OFFIS (D). Local Principal Investigator: prof. D. Sciuto.

2.6. PARTICIPATION TO NATIONAL RESEARCH PROJECTS

- Two-year scientific national inter-university co-funded research program **MIUR – PRIN 2005** (Prot. 2005095528) "Metodologie di progettazione di sistemi multiprocessore on-chip basati sul concetto di piattaforma" (Design methodologies of multiprocessor systems-on-chip based on the concept of platform). National Scientific Coordinator: prof. D. Sciuto (Politecnico di Milano).
- Two-year scientific national inter-university co-funded research program **MIUR–2002** (Prot. 2002092153) "Metodologie di progetto per sistemi digitali integrati su singolo chip di tipo embedded" (Design methodologies for single-chip embedded systems). National Scientific Coordinator: prof. M. Sami (Politecnico di Milano)
- National scientific research project **FIRB – MAIS – 2001** "Sistemi informativi adattativi multicanale" (Adaptive multi-channel computing systems). National Scientific Coordinator: prof. B. Pernici (Politecnico di Milano).
- Two-year scientific national research project: **CNR Italian Research Council - 1997-98** Project: "Metodologie e Strumenti per la Progettazione Automatica di Circuiti e Sistemi Digitali a Basso Consumo di Potenza". (Methodologies and Tools for the Automatic Design of Low-Power Digital Circuits and Systems). National Scientific Coordinator: Prof. M. Mezzalama, Politecnico di Torino.

2.7. PARTICIPATION TO INDUSTRIAL FUNDED RESEARCH PROJECTS

- **Participation** to the two-year research project: "Power estimation methodologies for VLIW architectures" (2000-2002) between DEI - Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics**, Agrate Brianza. Principal Investigator: prof. M. Sami. The activity carried out in this project has been the subject of **one patent granted** by the USA Dept. of Commerce, Patent and trademark Office [P4-US].

2.8. EVALUATION OF RESEARCH PROJECTS FOR THE EUROPEAN COMMISSION:

1. **Independent Expert Reviewer**, ARTEMIS JU – Project 295440 PaPP (Portable and Predictable Performance on heterogeneous embedded many-cores), 2013-2015.
2. **Independent Expert Reviewer**, FP7 – STREP Project 288570 ParaPhrase (Parallel Patterns for Adaptive Heterogeneous Multicore Systems), 2012-2014.
3. **Independent Expert Reviewer**, FP7 – STREP Project 248976 REFLECT (Rendering FPGAs to Multi-Core Embedded Computing), 2010-2012.
4. **Independent Expert Reviewer** to evaluate research proposals submitted to the "Future and Emerging Technologies" programme (EC FET-Open) on FP7-ICT-2009, 2010-2013.
5. **Independent Expert Reviewer** to participate in the on-site Evaluation Panel to evaluate research proposals submitted to the "Future and Emerging Technologies" programme (EC FET-Open) on FP7-ICT-2009 Batch 13, June 2012.
6. **Independent Expert Reviewer**, Network-of-Excellence Project FP6 - IST-4408 HiPEAC (High-Performance Embedded Architectures and Compilers) coordinated by prof. Mateo Valero, Universidad Politecnica de Catalunya, Barcelona. 2005-2008.
7. **Independent Expert Reviewer**, to participate to the on-site Evaluation Panel for the European IV Call IST (Information Society Technology) - FP6 (6th Framework Programme) on Nanoelectronics, April 2005.

2.9. EVALUATION OF RESEARCH PROJECTS FOR VARIOUS SCIENCE FOUNDATIONS

1. **Expert Reviewer**, Swiss National Science Foundation, Switzerland, 2016.
2. **Expert Reviewer**, Programme Blanc International Edition 2010, ANR (Agence Nationale de la Recherche), France, 2010.
3. **Chair of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering, 2009.
4. **Member of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering, 2008.
5. **Primary Evaluator**, INRIA (French National Institute for Computer Science - France), 2007..

3. SCIENTIFIC SERVICES

I am an active member of the research community, and so far I have organized several international conferences and workshops as Program Chair or General Chair and I regularly serve in several technical program committees.

3.1. ORGANIZING COMMITTEE MEMBER

1. **Track Chair**, Architectural and Microarchitectural Design, DATE 2017, IEEE/ACM Design and Test in Europe Conference, Lausanne (Switzerland), March 27-31, 2017.
2. **Program Co-Chair**, PARMA-DITAM Workshop 2017, co-located with HiPEAC 2017 Conference, Stockholm (Sweden), Jan. 25, 2017
3. **Track Chair**, Hardware for Embedded Systems, ICCAD2016, The IEEE/ACM International Conference on Computer-Aided Design 2016, Austin, Texas, USA, November 7-10, 2016
4. **Co-Organizer**, First Workshop on Resource Awareness and Application Autotuning in Adaptive and heterogeneous Computing (Res4Ant), co-located with DATE 2016, Dresden (Germany), March 18, 2016.
5. **Track Co-Chair**, Architectural and Microarchitectural Design, DATE 2016, IEEE/ACM Design and Test in Europe Conference, Dresden (Germany), March 14-18, 2016.
6. **General Co-Chair**, PARMA-DITAM Workshop 2016, co-located with HiPEAC 2016 Conference, Prague (Czech Republic), Jan. 18-20, 2016.
7. **Track Chair**, Embedded System Hardware, ICCAD2015, The IEEE/ACM International Conference on Computer-Aided Design 2015, Austin, Texas, USA, November 2-6, 2015.
8. **Local Organizer**, HiPEAC Computing System Week, held at Politecnico di Milano (Italy), September 21-23, 2015.
9. **Program Chair**, FPL 2015, 25th International Conference on Field Programmable Logic and Applications, London (UK), September, 2015.
10. Program Co-Chair, **ViPES'2015**, 3rd Workshop on Virtual Prototyping of Parallel and Embedded Systems, co-located with SAMOS Conference 2015, July 19th, 2015, Samos.
11. **Subcommittee Chair**, Embedded System Design, DAC 2015, 52nd ACM/IEEE Design Automation Conference, San Francisco CA, June 7-11, 2015.
12. **Track Co-Chair**, Architectural and Micro-architectural Design, DATE 2015, IEEE/ACM Design and Test in Europe Conference, Grenoble (France), March 9-13, 2015.
13. **General Co-Chair**, PARMA-DITAM Workshop 2015, co-located with HiPEAC 2015 Conference, Amsterdam (NL), January 19-21, 2015.
14. **Track Co-Chair**, Design Methods and Tools, FPL 2014, 24th International Conference on Field Programmable Logic and Applications, Munich (Germany), Sept., 2014.
15. **General Chair**, PARMA-DITAM Workshop 2014, co-located with HiPEAC Conference 2014, Wien (A), Jan. 20, 2014.
16. **Track Co-Chair**, SoC Design and Interconnect, VLSI-SOC 2013, 21st IFIP/IEEE International Conference on Very Large Scale Integration, Istanbul (Turkey), October, 2013.
17. **Workshops Co-Chair**, FPL 2013, 23rd International Conference on Field Programmable Logic and Applications, Porto, Sept. 2-4, 2013.
18. **General Co-Chair**, DEPCP 2013, 5th DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 22nd, 2013.
19. **General Co-Chair**, Fall School on Programming Paradigms for Multi-core Embedded Systems, Freudenstadt – Lauterbad, Germany, October 2-5, 2012.
20. **Program Co-Chair**, ASAP 2012, 23rd IEEE International Conference on Application-specific Systems, Architectures and Processors, Delft (NL), 9-11 July 2012.
21. **Subcommittee Co-Chair**, Embedded Systems Design Methodologies, DAC 2012, ACM/IEEE Design Automation Conference, San Francisco CA, 3-7 June 2012.
22. **General Co-Chair**, DEPCP 2012, 4th DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 16th, 2012.
23. **Co-Organizer**, RAPIDO Workshop 2012 on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2012, Paris.
24. **General Co-Chair**, DEPCP 2011, 3rd DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 18th, 2011.
25. **Program Co-Chair**, ARCS 2011, Architecture of Computing Systems Conference, Como (Italy), 22-25 Feb. 2011.

26. **Co-Organizer**, RAPIDO Workshop 2011, on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2011, Crete.
27. **Program Co-Chair**, SASP 2010, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference), Anaheim, CA, June 13-18, 2010.
28. **Co-Organizer** and **Architectures Session Chair**, DEPCP 2010, Second DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 12th, 2010.
29. **General Co-Chair**, PARMA Workshop 2010 on Parallel Programming and Run-time Management Techniques for Many-core Architectures, co-located with ARCS 2010 - Architecture of Computing Systems Conference, Hannover (D), February 2010.
30. **Co-Organizer**, RAPIDO Workshop 2010 on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2010, Pisa.
31. **General Co-Chair**, SASP 2009, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) San Francisco, CA, July 27-28, 2009.
32. **Program Co-Chair**, SAMOS IX Workshop on Systems, Architectures, Modeling and Simulation, Samos, Greece, July, 2009.
33. **Co-Organizer** and **Architectures Session Chair**, DEPCP 2009, First DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Nice, April 24th, 2009.
34. **General Co-Chair**, MICRO 2008, 41st Annual IEEE/ACM International Symposium on Microarchitecture, Como (Italy), 8-12 November 2008.
35. **Publicity Chair**, SASP 2008, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) Anaheim, CA, June 8-9, 2008.
36. **Publicity Chair**, WASP2007, Fifth Workshop on Application Specific Processors, 2007.

3.2. PROGRAM COMMITTEE MEMBER

1. **ARC 2017**, 13th International Symposium on Applied Reconfigurable Computing.
2. **IPDPS**, IEEE International Parallel and Distributed Processing Symposium, 2015, 2016.
3. **DAC**, ACM/IEEE Design Automation Conference, 2011-2013, 2015.
4. **DATE**, IEEE/ACM Design and Test in Europe Conference, 2005-2017.
5. **FPL**, International Conference on Field Programmable Logic and Applications, 2013-2016.
6. **ICCAD**, IEEE/ACM International Conference on Computer-Aided Design, 2014, 2015, 2017.
7. **NOCS**, ACM/IEEE International Symposium on Networks-on-Chip, 2009-2016.
8. **DSD**, Euromicro Conference on Digital System Design, 2012- 2016.
9. **ASAP**, IEEE International Conference on Application-specific Systems, Architectures and Processors, 2012-2016.
10. **ARCS**, Architecture of Computing Systems Conference, 2010-2014, 2017.
11. **IC-SAMOS**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2006-2017.
12. **HPCC**, IEEE International Conference on High Performance Computing and Communications, 2014.
13. **ICPP**, IEEE International Conference on Parallel Processing, 2011, 2013.
14. **EUC 2013**, IEEE/IFIP Int. Conf. on Embedded and Ubiquitous Computing, 2013.
15. **MES 2013**, International Workshop on Many-core Embedded Systems.
16. **VLSI-SOC**, IFIP/IEEE International Conference on Very Large Scale Integration, 2008-2011, 2013.
17. **HPCA-18**, 18th International Symposium on High Performance Computer Architecture, 2012.
18. **IA³**, Workshop on irregular Applications: Architectures and Algorithms, 2011-2012
19. **CF**, ACM International Conference on Computing Frontiers, 2009, 2012, 2016-2017.
20. **WRC**, Workshop on Reconfigurable Computing, co-located with HiPEAC Conference, 2010-2012.
21. **PDP**, Euromicro International Conference on Parallel, Distributed and Network-Based Computing, 2012
22. **SASP**, IEEE Symposium on Application Specific Processors, 2008-2011.
23. **MICRO-43**, 43rd Annual IEEE/ACM International Symposium on Microarchitecture, 2010.
24. **HiPEAC**, International Conference on High-Performance Embedded Architectures and Compilers, 2010.
25. **ICS**, the 20th ACM International Conference on Supercomputing, 2006.
26. **WASP**, Workshop on Application Specific Processors, 2004-2007.

3.3. ASSOCIATE/GUEST EDITOR AND JOURNAL REVIEWER

- **Associate Editor**, ACM Transactions on Architecture and Code optimization (TACO) (2015-present).
- **Associate Editor**, MICPRO Journal, Embedded Hardware Design (Microprocessor and Microsystems), Elsevier (2013- 2015)
- **Guest Co-Editor**, Special Issue with selected papers from FPL 2015, 25th International Conference on Field Programmable Logic and Applications, to be published in 2016 on ACM Transactions on Reconfigurable Technology and Systems (TRETS).
- **Guest Co-Editor**, Special Issue with selected papers from VIPES2015, to be published in 2016 on ACM Transactions on Embedded Computing Systems (TECS).
- **Guest Co-Editor**, Special Issue with selected papers from DSD2012 on Reliability and Dependability in MPSoC Technologies, Journal on Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), Elsevier, Vol. 37, Number 8-A, 2013 (09/2012 – 12/2012).
- **Selection Committee Member**, IEEE MICRO Special Issue on “Top Picks 2010 from Computer Architecture Conferences”, January/February 2011.
- **Guest Co-Editor**, Special Issue with selected papers from International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS2009) on Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), Volume 5, Issue 3, Springer. (09/2009 – 03/2010)
- **Subject Area Editor**, Journal of Systems Architecture – The EUROMICRO Journal, Elsevier Ed. (06/2003 - 10/2005).

From 1993 to present, I'm servicing as **reviewers** for several prestigious international journals such as: IEEE Transactions on Computers; IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems; IEEE Transactions on Very Large Scale Integration Systems; IEEE Design and Test; IEEE Micro; ACM Transactions on Design Automation of Electronic Systems; ACM Transactions on Embedded Computing Systems; Springer Journal on VLSI Signal Processing Systems; Springer Journal on Design Automation for Embedded Systems; Elsevier Journal on Microprocessors and Microsystems: Embedded Hardware Design (MICPRO); IET Computers and Digital Techniques;

3.4. INVITED TALKS, SEMINARS AND PANELS

1. June 9, 2016, "Design Space and Application Autotuning for Runtime Adaptivity in Multicore Architectures", **Seminar** at Brain Inspired Computing Group, IBM Research, Austin, Host: Dr. Jun Sawada, IBM Research, Austin.
2. June 3, 2016, "Design Space and Application Autotuning for Runtime Adaptivity in Multicore Architectures", **Seminar** at the University of Texas at Austin, Electrical and Computer Engineering, Computer Architecture Seminar Series, Austin, Host: prof. Andreas Gerstlauer, prof. Yale Patt, University of Texas at Austin, [Link](#)
3. May 17, 2016, **Panel Moderator** on: "Power Efficiency: Where are you?" Panelists: Adolfo Hoisie, Marek Michalewicz, Roberto Giorgi, Tobias Gemmeke, held at ACM International Conference on Computing Frontiers 2016, Como, Italy.
4. March 18, 2016, **Panel Moderator** on: "Moore's law is still alive! So why resource awareness?", Panelists: Cathal McCabe, Axel Auweter, João M. P. Cardoso, Axel Jantsch, X. Sharon Hu, Andreas Rohatschek and Michael Hübner; held at First Workshop on Resource Awareness and Application Autotuning in Adaptive and Heterogeneous Computing, co-located with DATE2016 Conference on Design , Automation and Test in Europe, Dresden, Germany.
5. October 21st, 2015, "Design Space Exploration and Application Autotuning for Runtime Adaptivity in Multicore Architectures" **Keynote Speaker** at the 13th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC2015) / 18th IEEE International Conference on Computational Science and Engineering (CSE2015), Porto (Portugal).
6. October 23rd, 2015, "ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems", **Invited Talk** at the Special Session on FET-HPC and Exascale Recently EU-funded projects, 13th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC2015) / 18th IEEE International Conference on Computational Science and Engineering (CSE2015), Porto (Portugal).
7. September 29-30, 2015, "ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems", **Invited Talk** at the ETP4HPC (European Technology Platform for High Performance Computing) - EXDCI (European eXtreme Data and Computing Initiative) Workshop, Rome (Italy).
8. September 21st, 2015, "ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems", **Invited Talk** at the Thematic Section on Challenges and opportunities in next-generation HPC Systems for Real-Time Applications, HiPEAC Computing System Week, Milan (Italy), Host: Prof. José Flich, Univ. Politècnica de València. SLIDES
9. October 8th, 2014, "Managing Adaptability in Heterogeneous Architectures through Performance Monitoring

- and Prediction", **Invited Talk** at the Thematic Section on Heterogeneous System Tools for Simulation, Debugging, Performance Modeling and Resource Management, HiPEAC Computing System Week, Athens, Host: Prof. Georgios Goumas, National Technical University of Athens.
10. May 15th, 2014, "Managing Adaptability in Dynamically Reconfigurable Architectures through Performance Monitoring and Prediction", **Invited Talk** at the Thematic Section on Reconfigurable Computing, HiPEAC Computing System Week, Barcelona, Host: Prof. Georgi Gaydadjiev, Chalmers University of Technology.
 11. September 4th, 2013, **Panel Moderator** on: "EU Horizon 2020 on Reconfigurable Computing" Invited Speakers: Dr. Panos Tsarchopoulos, Future and Emerging Technologies, EU Project Officer; Dr. Georgi Kuzmanov, ARTEMIS Joint Undertaking, EU Programme Officer; held at FPL2013, 23rd International Conference on Field Programmable Logic and Applications, Porto.
 12. June 8th, 2012, "Automatic Design Space Exploration for Multi-core Architectures", **Seminar** at Intel Labs, Santa Clara (CA, USA), Host: Dr. Akhilesh Kumar, Intel.
 13. April 25th, 2012. "Design-time support for run-time management of embedded multiprocessor architectures", **Invited Talk** at the Thematic Section on Design and runtime management of reconfigurable systems, HiPEAC Computing System Week, Goteborg, Host: Prof. Georgi Gaydadjiev, Chalmers University of Technology.
 14. February 7th, 2012, "Design Space Exploration and Run-time Resource Management for Multi-core Architectures", **Seminar** at the University of Texas at Austin, Electrical and Computer Engineering, Computer Architecture Seminar Series, Austin, Host: Prof. Yale Patt, University of Texas at Austin.
 15. September 7th, 2011, "2PARMA Project" **Invited Talk** at FPL2011 European Project Workshop, Chania, Crete. Organizer. Prof. Joao Cardoso, Univ. of Porto.
 16. April 7th, 2011, "2PARMA Project: PARallel PARadigms and Run-time MANagement techniques for Many-core Architectures", **Invited Talk**, HiPEAC Cluster Meeting on Multi-core Architectures, 2011 Chamonix (F), Host: Prof. Per Stenström, Chalmers University of Technology.
 17. November 24th, 2010, "Automatic Design Space Exploration for Chip Multi-processors", **Invited Talk** at the Workshop on "Challenges in Embedded System Design": Involvement of SMEs in Designing Complex Systems (CMM 2010), University of Lugano (CH), Workshop Organizers: Prof. G. De Micheli (EPFL) and Prof. M. Sami (USI-Politecnico di Milano).
 18. July 6th, 2010, "MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures", **Invited Talk** at the Research Projects Workshop at ISVLSI 2010: IEEE Computer Society Annual Symposium on VLSI, July 5-7, 2010, Lixouri Kefalonia, Greece.
 19. June 18th, 2010, "Automatic Design Space Exploration for Chip-Multi Processors". **Seminar** at University of California Riverside, Department of Computer Science & Engineering, Riverside (CA, USA), Host: Prof. Walid Najjar, University of California Riverside.
 20. June 17th, 2010, "Automatic Design Space Exploration for Chip-Multi Processors". **Seminar** at University of California Irvine, Department of Computer Science & Engineering, Irvine (CA, USA), Host: Prof. Alexander V. Veidenbaum, University of California Irvine.
 21. March 23rd, 2010, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "A Design Space Exploration Framework for Run-Time Resource Management on Multi-Core Architectures". Host: Prof. Koen Bertels, Delft Technical University.
 22. December 17th, 2009, **Seminar** at NEC Laboratories America, Inc., Princeton Campus, Princeton (NJ - USA), Title: "Automatic Design Space Exploration for Chip-Multi Processors". Host: Dr. Marcello Lajolo, NEC Labs America.
 23. December 16th, 2009, **Seminar** at Princeton University, Department of Electrical Engineering, Computer Engineering Seminar, Title: "Automatic Design Space Exploration for Chip-Multi Processors", Host: Prof. Ruby Lee, Princeton University.
 24. July 29th, 2009, **Seminar** at HP Labs, Palo Alto, Title: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs", Host: Dr. Matteo Monchiero, HP Labs, Palo Alto.
 25. May 14th, 2009, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs" Host: Prof. Koen Bertels, Delft Technical University.
 26. April 25th, 2006, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "Exploration and Optimization of Multiprocessor Embedded Architectures based on Networks-on-Chip", Host: Prof. Stamatis Vassiliadis, Delft Technical University.
 27. September 22nd, 2005, New York, USA, **Panelist at WASP 2005** Workshop on Application Specific Processors (co-located with International Conference on Hardware/Software Codesign and System Synthesis), Panel title: "Application Specific Customizations: Processor or System Level?" Moderator: Prof. Daniel Gajski, UC Irvine.

3.5. MEMBER OF PROFESSIONAL ORGANIZATIONS

- Since 2013, **Member** of ACM (Association of Computing Machinery).
- Since 1993, **Member** of IEEE (Institute of Electrical and Electronics Engineers), **Senior Member** effective from August 2009, **IEEE Fellow** effective from January 2017.
- Since 2008, **Member** of HiPEAC Network of Excellence.

4. ACADEMIC SERVICES

4.1. TEACHING ACTIVITIES AT UNIVERSITIES

With respect to teaching, I have balanced my efforts in the past years in teaching both at the Undergraduate level and at the Master of Science level at Politecnico di Milano and previously at the Università degli Studi di Milano. At the Undergraduate level, I have covered several courses in the Computer Engineering track: Computer Architectures, Operating Systems, Logic Design and Computer Science Fundamentals. At the M. Sc. level, I have taught courses mainly related to my research areas: Advanced Computer Architectures and Hardware/Software Co-design Methodologies. I have an extensive **English-speaking teaching experience** in a multicultural environment thanks to my courses at the M.Sc. program in Computer Engineering at the Como Campus of Politecnico di Milano (2003-present) and at the Università della Svizzera Italiana (2012). From 2002 to present, I was **advisor of more than 60 M.Sc. students** in Computer Engineering at Politecnico di Milano. Since 20002, I was member of several Thesis Committees at the Undergraduate and M. Sc. level in Computer Engineering at Politecnico di Milano. Apart from course developments, **I enjoy teaching and I have a strong commitment to teach topics related to Computer Architectures**. My efforts are devoted to directly transfer to the students my research knowledge and results not only through continuously updating the concepts exposed in the courses to reflect state-of-the-art concepts, but also during the advising of the students for the development of course projects and M.Sc. thesis. This process is to make sure the students are aware of the state-of-the-art research on computer architectures and related tools. It is also important to have a constructive and continuous interaction with the students and to allow them to contribute to the improvements and quality assessment in teaching. I believe top quality teaching and good international visibility are key issues to guarantee adequate levels of in-flow of high quality students. A way to enhance the industrial exposure of our M.Sc. students is by offering internships during which they can work on industrial projects. In the past years, I have followed several students doing an internship (in the context of their Master thesis) with STMicroelectronics. Furthermore, I am **co-author of the academic textbook** (in Italian): "Progettazione digitale" (Logic Design) edited by McGraw-Hill, First Edition 2002, Second Edition 2007. The textbook is currently used at the undergraduate level in basic courses of Logic Design in Computer Engineering and Computer Science tracks.

2016/2017

- "Architettura dei Calcolatori e Sistemi Operativi (II Modulo)" (5 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2016.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2017.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus (Course completely offered in English), Spring 2017.

2015/2016

- "Architettura dei Calcolatori e Sistemi Operativi (II Modulo)" (5 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2015.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2016.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus (Course completely offered in English), Spring 2016.

2014/2015

- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2015.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus (Course completely offered in English), Spring 2015.

2013/2014

- "Architettura dei Calcolatori e Sistemi Operativi (I Modulo)" (5 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2013.
- "Architetture Avanzate dei Calcolatori" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2013.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English) , Spring 2014

2012/2013

- "Architettura dei Calcolatori e Sistemi Operativi (I Modulo)" (5 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2012.
- "Advanced Computer Architectures" (3 Credits), Master of Science, Embedded System Design, Università della Svizzera Italiana, Lugano (Course completely offered in English), Fall 2012.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano,

Como Campus (Course completely offered in English), Spring 2013.

2011/2012

- "Architettura dei Calcolatori e Sistemi Operativi" (10 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2011.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2012.

2010/2011

- "Architettura dei Calcolatori e Sistemi Operativi" (10 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2010.
- "Advanced Computer Architectures" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2011.

2009/2010

- "Architettura dei Calcolatori e Sistemi Operativi" (10 Credits), Undergraduate Programme, Computer Engineering, Politecnico di Milano, Como Campus, Fall 2009.
- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2010.

2008/2009

- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2008.
- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2009.

2007/2008

- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2007.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2007.
- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2008

2006/2007

- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2006.
- "Informatica A " (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2006.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2007.
- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2007.
- "Advanced Computer Architectures", (2.5 Credits) Ph. D. Programme, Computing Systems Engineering, Politecnico di Milano, Milano Leonardo Campus (in collaboration with prof. M. Sami), Spring 2007.

2005/2006

- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2005.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2005.
- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus (Course completely offered in English), Spring 2006.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2006.

2004/2005

- "Metodologie di progetto hardware/software" (5 Credits), Master of Science, Computing Systems Engineering and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Fall 2004.
- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2004.
- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus, Spring 2005.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2005.

2003/2004

- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di

Milano, Como Campus, Fall 2003.

- "Architectures for Multimedia Systems" (5 Credits), Master of Science, Computer Engineering, Politecnico di Milano, Como Campus, Spring 2004.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2004.

2002/2003

- "Informatica A" (10 Credits), Undergraduate Programme, Management and Production Engineering, Politecnico di Milano, Como Campus, Fall 2002.
- "Calcolatori Elettronici" (10 Credits), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2003.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2003.

2001/2002

- "Computer Architectures I" (Labs for prof. N. Scarabottolo), Undergraduate Programme, Computer Science, University of Milan, Crema Campus, Fall 2001.
- "Calcolatori Elettronici" (10 Credits), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2002.
- "Architettura degli Elaboratori e delle Reti" (12 Credits), Undergraduate Programme, Information and Communication Technology, University of Milan, Spring 2002.

2000/2001

- "Architettura degli Elaboratori I" (Labs for prof. N. Scarabottolo), Undergraduate Programme, Computer Science, University of Milan, Crema Campus, Fall 2000.
- "Architettura degli Elaboratori e delle Reti / Il Modulo" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Spring 2001.
- "Laboratorio di Sistemi Operativi / I Modulo" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Spring 2001.
- "Advanced Computer Architectures" (3 Credits), Ph. D. Programme, Computer Science, Department of Computer Science, University of Milan, Spring 2001.
- "Calcolatori Elettronici" (Labs for prof. M. Sami), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2001.

1999/2000

- "Laboratorio di Architettura degli Elaboratori I" (6 Credits), Undergraduate Programme, Computer Science, University of Milan, Crema Campus, Fall 1999.
- "Calcolatori Elettronici" (Labs for prof. M. Sami), Master of Science, Electronics and Telecommunications Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2000.
- "Calcolatori Elettronici" (Labs for prof. R. Stefanelli), Master of Science, Computer Engineering, Politecnico di Milano, Milano Leonardo Campus, Spring 2000.

4.2. **ACADEMIC RESPONSIBILITIES**

Since 2002, I am an active and permanent contributor to the organisation of the teaching activities and tracks in Computer Engineering at Politecnico di Milano, Como Campus, where I have had several responsibilities and I was participating to a number of committees:

- **Chair**, Committee on Undergraduate Study Plans (Commissione Piani degli Studi Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2002-Present.
- **Chair**, Committee on Undergraduate Transfers (Commissione Passaggi e Trasferimenti Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- **Member**, Committee on Graduate Admissions (Commissione Ammissioni alla Laurea Magistrale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- **Member**, Committee on Undergraduate Studies (Commissione Didattica Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.

After the recent merging of the organisation of Computer Engineering tracks in Como Campus and Milano Leonardo Campus, I have started to participate to the following committees:

- **Member**, Committee on Graduate Admissions (Commissione Ammissioni alla Laurea Magistrale) in Computer Engineering, Politecnico di Milano, 2015-Present.

I have also been part of the following temporary committees:

- **Member**, Committee for the comparative evaluation of the candidates for the position of Temporary Researcher (Ricercatore Temporaneo) in Computer Engineering, Politecnico di Milano, 2010.
- **Member**, Committee for the comparative evaluation of the candidates for one position as Assistant Professor (Ricercatore MIUR) in Computer Engineering, University of Catania, 2007-2008.

4.3. RESEARCH ADVISING

4.3.1. Doctoral Students Supervision

1. **Vittorio Zaccaria**, Ph. D. 2002, Politecnico di Milano. Currently Assistant Professor at Politecnico di Milano, DEIB. First employment: R&D Engineer at STMicroelectronics. Ph.D. Thesis on: "Power exploration methodologies for VLIW-based systems", Advisor: prof. M. Sami. Co-advisors: prof. D. Sciuto, Dr. C. Silvano.
2. **Gianluca Palermo**, Ph.D. 2006, Politecnico di Milano. Currently Associate Professor at Politecnico di Milano, DEIB. First employment: Post-Doctoral Researcher at Politecnico di Milano. Ph.D. Thesis on: "Design Methodologies for Embedded Architectures based on Network on-Chip", Advisor: prof. C. Silvano.
3. **Giovanni Beltrame**, Ph.D. 2006, Politecnico di Milano. Currently Assistant Professor at École Polytechnique de Montréal. First employment: Microelectronics Engineer at European Space Agency (NL). Ph.D. Thesis on "Modeling, Simulating, Analysis and Optimization of Multi-Processor System-on-Chip Platforms", Advisor: prof. D. Sciuto. Co-advisor: prof. C. Silvano.
4. **Matteo Monchiero**, Ph.D. 2007, Politecnico di Milano. Currently Senior Research Scientist, Intel Labs at Santa Clara (CA, US). First employment: Post-Doctoral Research Associate at HP Labs in Palo Alto, Exascale Computing Lab., Ph.D. Thesis on: "Power/performance analysis and optimization of multicore architectures", Advisor: prof. C. Silvano.
5. **Oreste Villa**, Ph.D. 2008, Politecnico di Milano. Currently Senior Research Scientist, at NVIDIA (CA). First employment: Research Scientist at Pacific Northwest National Laboratory, Richland, WA (USA), Ph.D. Thesis: "Designing and Programming Multi-core Architectures", Advisor: prof. C. Silvano.
6. **Giovanni Mariani**, Ph. D. 2011, Università della Svizzera Italiana (USI). Currently Post-Doctoral Researcher at ASTRON & IBM Center of Exascale Technology (NL). First employment Post-Doc at ALaRI - USI (CH) and Associate Researcher at TU Delft(NL). Ph.D. Thesis: "A Design Space Exploration Methodology Supporting Run-time Resource Management for Multi-Core Architectures", Advisor: prof. M. Sami, Co-advisor: prof. C. Silvano
7. **Leandro Fiorin**, Ph. D. 2012, Università della Svizzera Italiana (USI). Currently Post-Doctoral Researcher at ASTRON & IBM Center for Exascale Technology (NL). First employment: Post-Doc at ALaRI –USI (CH). Ph.D. Thesis: "High level services for Networks-on-Chip", Advisor: prof. M. Sami, Co-advisor: prof. C. Silvano.
8. **Edoardo Paone**, Ph. D. 2014, Politecnico di Milano, DEIB, XXVII cycle. Currently Embedded Software Engineer at Ericsson (Sweden). Ph.D. Thesis: "Design Space Exploration of OpenCL Applications on Heterogeneous Parallel Platform". Ph.D. defense held in Dec. 2014. Advisor: prof. C. Silvano.
9. **Ioannis Stamelakos**, Ph. D. student at Politecnico di Milano, DEIB, XXVIII cycle. Ph.D. Thesis: "Near-Threshold Computing with Performance Guarantees for Manycore Architectures". Ph.D. defense expected in Dec. 2016. Advisor: prof. C. Silvano. Co-advisor: Dr. S. Xydis, NTUA.
10. **Amir Hossein Ashouri**, Ph. D. student at Politecnico di Milano, DEIB, XXVIII cycle. Ph.D. Thesis: "Compiler Autotuning using Machine Learning Techniques". Ph.D. defense expected in Dec. 2016. Advisor: prof. C. Silvano, Co-Advisors: prof. G. Palermo, Prof. John Cavazos.
11. **Davide Gadioli**, Ph. D. student at Politecnico di Milano, DEIB, XXIX cycle. Ph.D. Thesis: "Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications". Ph.D. defense expected in 2017. Advisor: prof. C. Silvano. Co-advisor: prof. G. Palermo.
12. **Ahmet Erdem**, Ph. D. student at Politecnico di Milano, DEIB, XXXII cycle. Ph.D. Thesis: "Hybrid Multiprocessor Architectures and Tools for Deep Learning and Convolutional Neural Network Applications". Ph.D. defense expected in 2020. Advisor: prof. C. Silvano. Co-advisor: Dr. G. Desoli, STMicroelectronics.

4.3.2. Undergraduate and Master Students Supervision

- Advisor of more than **60** Master students in Computer Engineering, Electrical Engineering, and Communication Engineering at Politecnico di Milano, 2002-Present.
- Advisor of some undergraduate and Master students in Computer Science at Università degli Studi di Milano, 2000-2002.
- Co-advisor of some Master students in Electrical Engineering at Università degli Studi di Brescia, 1996-1999.
- Advisor / co-advisor of some Master students in Information Technology at CEFRIEL Research and Training Center in Milano, EDA (Electronic Design Automation) Group, 1993-1999.

4.4. PHD EXTERNAL EXAMINER

- In November 2016, I have been invited as Opponent Member of the Doctoral Examination Committee, Rheinisch-Westfaalischen Technischen Hochschule Aachen (Germany), for the Ph.D. defense of the candidate **Daniel Guenther** discussing a thesis titled: "Hardware and Software Design Methodologies for Portability, Flexibility and Versatility in Multi-Standard MIMO Baseband Processing", Advisors: prof. Gerd Ascheid.
- In November 2014, I have been invited as Opponent Member of the Doctoral Examination Committee, Eindhoven University of Technology (NL), for the Ph.D. defense of the candidate **Dongrui She** discussing a thesis titled: "Energy Efficient Code Generation for Streaming Applications", Advisors: prof. Henk Corporaal.
- In April 2013, I have been invited as Opponent Member of the Doctoral Examination Committee, Technical University of Catalonia UPC (Spain) for the Ph.D. defense of the candidate **Nikita Nikitin** discussing a thesis titled: "Automatic Synthesis and Optimization of Chip Multiprocessors", Advisors: prof. Jordi Cortadella.
- In June 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, Technical

University of Catalonia – UPC (Spain) for the Ph.D. defense of the candidate **Friman Sánchez Castaño** discussing a thesis titled: "Exploiting Multiple Levels of Parallelism in Bioinformatics Applications", Advisors: prof. Alex Ramírez and prof. Mateo Valero.

- In April 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, University of Verona, for the Ph. D. defense of the candidate **Francesco Stefanni** discussing a thesis titled: "A design and verification methodology for networked embedded systems", Advisor: prof. Franco Fummi.
- In February 2011, I have been invited as Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate **Kamana Sigdel** discussing a thesis titled: "System-level Design Space Exploration of Reconfigurable Architectures". Advisors: prof. K. Bertels and prof. A. Pimentel.
- In May 2009, I have been invited as Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate **Carlo Galuzzi** discussing a thesis titled: "Automatically fused instructions". Advisor: prof. K. Bertels.

4.5. VISITORS

1. **Sotirios Xydis, Ph.D.**, currently Post-Doctoral Researcher at National Technical University of Athens; **Post-Doctoral Researcher** in my group at Politecnico di Milano (From Nov. 2011 to July 2013). His current research focuses on design space exploration, high level synthesis and programmable architectures
2. Arpad Gellért, Ph. D., Assistant Professor, "Lucian Blaga" University of Sibiu, Romania, Advisor: Prof. Lucian Vintan. **Visiting Researcher**, Spring 2009.
3. **Caroline Concatto**, Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 15-01-10 to 15-04-10 , FP7 HiPEAC NoE Collaboration Grant.
4. **Debora Matos**, Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 02-02-11 al 02-05-11, FP7 HiPEAC NoE Collaboration Grant.
5. **Anelise Kologeski**, Ph. D. student at Universidade Federal do Rio Grande do Sul, Instituto de Informática, Departamento de Informática Aplicada, Porto Alegre (Brasil). Advisor: Prof. Luigi Carro. **Visiting student** from 02-02-11 al 02-05-11, FP7 HiPEAC NoE Collaboration Grant.

5. LIST OF PATENTS AND AWARDS

5.1. PATENTS

Inventor/Co-inventor of **11** patent applications with Bull HN Information Systems and STMicroelectronics (**7 out of 11 already granted**):

- Integrated CMOS static RAM, EU Patent # [EP0578900 \(B1\)](#) [P1-EU] Granted 1997, DE Patent # [DE69223046 \(T2\)](#) [P1-DE] Granted 1998. Applicant: Bul HN Information Systems (IT)
- Digital information error correcting apparatus for single error correcting (SEC), double error detecting (DED), single byte error detecting (SBED), and odd numbered single byte error correcting (OSBEC), US Patent # [US5535227 \(A\)](#) [P2-US] Granted 1996. EU Patent # [EP0629051 \(B1\)](#) [P2-EU] Granted 1998, DE Patent # [DE69317766 \(T2\)](#) [P2-DE] Granted 1998. Applicant: Bul HN Information Systems (IT).
- Encoder/decoder architecture and related processing system, US Patent # [US20020019896 \(A1\)](#) [P3-US] Filed 2002. Encoder architecture for parallel busses, EU Patent # [EP1150467 \(A1\)](#) [P3-EU] Filed 2001. Applicant: ST Microelectronics (IT)
- Processor architecture US Patent # [US6889317 \(B2\)](#) [P4-US] Granted 2005. Processor architecture with variable-stage pipeline, EU Patent # [EP1199629 \(A1\)](#) [P4-EU] Filed 2002. Applicant: ST Microelectronics (IT)
- Programmable data protection device, secure programming manager system and process for controlling access to an interconnect network for an integrated circuit. US Patent # [US8185934 \(B2\)](#) [P5-US] Granted 2012. EU Patent # [EP2043324 \(A1\)](#) [P5-EU] Filed 2009. Applicant: STMicroelectronics Grenoble (F)

5.2. AWARDS

- Elevated to **IEEE Fellow** by the IEEE Board of Directors (effective from 2017) "*for contributions to energy-efficient computer architectures*". The IEEE Grade of Fellow is conferred by the IEEE Board of Directors upon a person with an outstanding record of accomplishments in any of the IEEE fields of interest. The total number selected in any one year cannot exceed the 0.1% of the total voting membership. IEEE Fellow is the highest grade of membership and is recognized by the technical and scientific community as a prestigious honor and an important career achievement
- **HiPEAC 2010 Paper Award**, given by the Steering Committee of the HiPEAC Network of Excellence as co-author of the paper: "A Correlation-Based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip " by G. Mariani, G. Palermo, V. Zaccaria, A. Brankovic, J. Jovic, C. Silvano. In Proceedings of **DAC-47** - Design Automation Conference, Anaheim, CA, USA, June 2010, pp. 120-125 url: <http://www.hipeac.net/award>
- In 2008, the paper titled: "Address Bus Encoding Techniques for System-Level Power Optimization", by L. Benini, G. De Micheli, E. Macii, D. Sciuto, C. Silvano, **DATE-98** [C82] has been recognized as one of **the most influential papers** of the past ten years DATE and then selected to be re-published as a chapter of the volume: **Design, Automation, and Test in Europe - The Most Influential Papers of 10 Years DATE** Lauwereins, Rudy; Madsen, Jan (Eds.), 2008.
- **ACM Recognition of Service Award**, given in Appreciation for Contributions to ACM as General Co-Chair MICRO-41: The 41st Annual IEEE/ACM Int. Symposium on Microarchitecture, Nov. 8-12, 2008.
- **Best Paper Award SAC 2008**, given at the 23rd Annual ACM Symposium on Applied Computing (Applications Theme) as co-author of the paper: M. Sykora, G. Agosta e C. Silvano, "Dynamic Configuration of Application Specific Implicit Instructions for Embedded Pipelined Processors", Fortaleza, Brazil, 16-20 March, 2008 [C45].
- **Bull Technical Award 1991**, given by Bull HN Information Systems for my contribution to the project: "*Integrated CAD framework for complex ASIC design*". The award has been motivated by my contribution to the solution to relevant technical problems demonstrating high professional competences, originality approach and constant personal commitment.

6. LIST OF PUBLICATIONS

6.1. INTERNATIONAL JOURNALS WITH PEER REVIEW

2016

- [J1]. Amir Hossein Ashouri, Giovanni Mariani, Gianluca Palermo, Eunjung Park, John Cavazos, Cristina Silvano, "COBAYN: Compiler Autotuning Framework Using Bayesian Networks", **ACM Transactions on Architecture and Code Optimization (TACO)**, Vol. 13, No. 2, Article 21, June 2016, [DOI](#)

2015

- [J2]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "DeSpErate++: An Enhanced Design Space Exploration Framework using Predictive Simulation Scheduling", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Vol. 34, No. 2, February 2015. pp. 293-306. [DOI](#)
- [J3]. Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High Level Synthesis", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Vol. 34, No. 1, January 2015, pp 155-159. [DOI](#)

2014

- [J4]. Leandro Fiorin, Gianluca Palermo and Cristina Silvano. "A Configurable Monitoring Infrastructure for NoC-Based Architectures", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**. Vol. 22, No. 11, November 2014, pp. 2436-2440, [DOI](#)

2013

- [J5]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "Design Space Exploration and Run-time Resource Management for Multi-cores", **ACM Transactions on Embedded Computing Systems (TECS)**, Vol. 13, Issue 2, Special Issue on Application Specific Processors, September 2013, pp. 20:1-20:27 [DOI](#)
- [J6]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "ARTE: An Application-specific Run-Time management framework for multi-cores based on queuing models", **Parallel Computing, Elsevier Journal**, Vol. 39, Issue 9, September 2013, pp. 504-519 Available online 20 April 2013, ISSN 0167-8191, [DOI](#)

2012

- [J7]. Andrea Di Biagio, Giovanni Agosta, Cristina Silvano and Martino Sykora, "Architecture Optimization of Application-Specific Implicit Instructions". **ACM Transactions on Embedded Computing Systems (TECS)**, Vol. 11, Issue S2, Article No. 44 (August 2012), pages 44:1 --44:23 (23 pages), [DOI](#)
- [J8]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria, "A Variability-Aware Robust Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints". **ACM Transactions on Embedded Computing Systems (TECS)**, Vol. 11, Issue 2, Article 29 (July 2012), pages 29:1 --29:28 (28 pages). [DOI](#)
- [J9]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Space", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Vol. 31, No. 5, May 2012, pp. 740-753, [DOI](#)

2011

- [J10]. Chantal Ykman-Couvreur, Prabhat Avasare, Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Linking run-time resource management of embedded multi-core platforms with automated design-time exploration", **IET Computers and Digital Techniques**, March 2011, Vol. 5, Issue 2, pp. 123-135 [DOI](#)

2009

- [J11]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "ReSPIR: A Response Surface-Based Pareto Iterative Refinement for Application-Specific Design Space Exploration", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Vol. 28, No. 12, Dec. 2009, pp. 1816-1829, [DOI](#)

2008

- [J12]. Leandro Fiorin, Gianluca Palermo, Slobodan Lukovic, Valerio Catalano, Cristina Silvano, "Secure Memory Accesses on Networks-on-Chip", **IEEE Transactions on Computers**, Vol. 57, No. 9, pp. 1216-1229, Sept., 2008, ISSN: 0018-9340, [DOI](#)

2007

- [J13]. Giovanni Beltrame, Donatella Sciuto, Cristina Silvano, "Multi-Accuracy Power and Performance Transaction-Level Modeling", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume: 26, No. 10, October 2007, Pages: 1830 -1842, [DOI](#)
- [J14]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors", **Journal of Systems Architecture: The Euromicro Journal - Elsevier**, Volume 53, Number 10, October 2007, pp. 719-732, [DOI](#)
- [J15]. Cristina Silvano, Giovanni Agosta, Gianluca Palermo, "Efficient Architecture/Compiler Co-Exploration Using Analytical Models", **Design Automation for Embedded Systems**, Springer, Volume 11, Issue 1, March 2007, pp. 1-23, ISSN

0929-5585 (Print) 1572-8080 (Online), DOI: 10.1007/s10617-006-9588-7, [DOI](#)

2006

- [J16]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Efficient Synchronization for Embedded on-Chip Multiprocessors", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Vol. 14, No. 10, October 2006, pp. 1049-1062, [DOI](#)

2005

- [J17]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "An Efficient Synchronization Technique for Multiprocessor Systems on-Chip". **ACM SIGARCH Computer Architecture News** (ACM, New York, USA) Volume 34, Issue 1 (March 2006) pp. 33-40. ISSN: 0163-5964, Special Issue on MEDEA-05 - International Workshop on MEMory performance: DEaling with Applications, systems and architecture" [DOI](#)
- [J18]. Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria, "Multi-Objective Design Space Exploration of Embedded Systems", **Journal of Embedded Computing, IOS Press**, Vol. 1, No. 3, 2005, pp. 305-316, ISSN 1740-4460, [url](#)
- [J19]. Andrea Bona, Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Reducing the Complexity of Instruction-Level Power Models for VLIW Processors", **Design Automation for Embedded Systems**, Springer US, March 2005, Vol. 10, No. 1, pp. 49-67, [DOI](#)
- [J20]. Matteo Monchiero, Gianluca Palermo, Mariagiovanna Sami, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Low-Power Branch Prediction Techniques for VLIW Architectures: A Compiler-Hints Based Approach", **Integration, The VLSI Journal**, Elsevier, Volume 38, Issue 3, January 2005, pp. 515-524, [DOI](#)

2002

- [J21]. Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Low-Power Data Forwarding for VLIW Embedded Architectures", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Vol. 10, No. 5, October 2002, Pages: 614 – 622, [DOI](#)
- [J22]. Luca Benini, Davide Bruni, Mauro Chinosi, Cristina Silvano, Vittorio Zaccaria, and Roberto Zafalon, "A Framework for Modeling and Estimating the Energy Dissipation of VLIW-based Embedded Systems", **Design Automation for Embedded Systems**, Kluwer Academic Publishers, Boston, October 2002, Volume 7, Issue 3, Pages: 183-203, [DOI](#)
- [J23]. Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria, "An Instruction-Level Energy Model for Embedded VLIW Architectures", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, Volume: 21, Issue: 9, Sept. 2002, Pages: 998 -1010, [DOI](#)
- [J24]. William Fornaciari, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria, "A Sensitivity-Based Design Space Exploration Methodology for Embedded Systems", **Design Automation for Embedded Systems**, Vol. Special Issue on "Design Methodologies and Tools for Real-Time Embedded Systems", Kluwer Academic Publishers, Boston, Sept. 2002, Volume 7, Issue 1-2, Pages: 7-33, [DOI](#)

1998

- [J25]. Franco Fummi, Donatella Sciuto, Cristina Silvano, "Automatic Generation of Error Control Codes for Computer Applications", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Vol. 6, No. 3, Sept. 1998, pp. 502-506, [DOI](#)
- [J26]. William Fornaciari, Paolo Gubian, Donatella Sciuto, Cristina Silvano, "Power Estimation of Embedded Systems: a Hardware/Software Co-design Approach", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Vol.6, No. 2, Jun. 1998, pp. 266-275, [DOI](#). This work has been selected to be re-published as Chapter 3 of the book: "Readings in Hardware/Software Co-design", Edited by G. De Micheli, R. Ernst, and W. Wolf, The Morgan Kaufmann Series in Systems on Silicon, Jun. 2001, ISBN 1-55860-702-1.

1997

- [J27]. William Fornaciari, Paolo Gubian, Donatella Sciuto, Cristina Silvano, "A VHDL-based Approach for Power Estimation of Embedded Systems", **Journal of System Architecture: The Euromicro Journal**, Volume 44, Issue 1, October 1997, pp. 37-61, [DOI](#)

1995

- [J28]. Luca Penzo, Donatella Sciuto, Cristina Silvano, "Construction Techniques for Systematic SEC-DED Codes with Single Byte Error Detection and Partial Correction Capability for Computer Memory Systems", **IEEE Transactions on Information Theory**, Vol. 41, No. 2, Mar. 1995, pp. 584-591, [DOI](#)

6.2. INTERNATIONAL BOOKS

- [B1]. Michael Huebner, Cristina Silvano, (**Editors**), "Near Threshold Computing. Technology, Methods and Applications", Springer, 1st Edition, 2016, IX, 100 p. 56 illus., Hardcover ISBN: 978-3-319-23388-8.
- [B2]. Cristina Silvano; Marcello Lajolo; Gianluca Palermo; (**Editors**), "Low-Power Networks- on-Chip", Springer, 1st Edition., 2011, X, 300 p. 100 illus., Hardcover ISBN: 978-1-4419-6910-1.
- [B3]. Cristina Silvano; William Fornaciari; Eugenio Villar; (**Editors**), "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Springer, 1st Edition, 2011, XVIII, 222, p. 88 illus.

Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011

- [B4]. Vittorio Zaccaria, Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano (**Authors**), "Power Estimation and Optimization Methodologies for VLIW-Based Embedded Systems", Kluwer Academic Publishers, Boston, Hardbound, ISBN 1-4020-7377-1, February 2003, 201 pp.

6.3. EDITORIAL CONTRIBUTIONS

- [E1]. Joao Cardoso and Cristina Silvano (**Guest Co-Editors**), Special Issue with selected papers from FPL 2015, 25th International Conference on Field Programmable Logic and Applications, *to be published in 2016* on ACM Transactions on Reconfigurable Technology and Systems (TRETS).
- [E2]. Jeronimo Castrillon and Cristina Silvano (**Guest Co-Editors**), Special Issue with selected papers from ViPES2015, *to be published in 2016* on ACM Transactions on Embedded Computing Systems (TECS).
- [E3]. Cristina Silvano, Walter Stechele, Stephan Wong, Jerónimo Castrillón, Michael Hübner, Amir Hossein Ashouri (**Editors**), Proceedings of the 1st International Workshop on REsource Awareness and Application Auto-tuning in Adaptive and heterogeNeous compuTing, co-located with 19th International Conference on Design, Automation And Test In Europe (DATE 2016), Dresden, Germany, March 18th, 2016. Series CEUR Workshop Proceedings, Vol. 1643, CEUR-WS.org Publisher, 2016, [URL](#)
- [E4]. Cristina Silvano, João M. P. Cardoso, Giovanni Agosta, Michael Hübner (**Editors**), Proceedings of the 7th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 5th Workshop on Design Tools and Architectures For Multicore Embedded Computing Platforms, PARMA-DITAM 2016, Prague, Czech Republic, January 18, 2016. ACM 2016, ISBN 978-1-4503-4052-6, [DOI](#)
- [E5]. Peter Y. K. Cheung, Wayne Luk and Cristina Silvano (**Editors**), Preface, 25th International Conference on Field Programmable Logic and Applications, FPL 2015, London, United Kingdom, September 2-4, 2015, pages 1-2, DOI 10.1109/FPL.2015.7293746.
- [E6]. Philip H. W. Leong, Hideharu Amano, Jason Anderson, Koen Bertels, João M. P. Cardoso, Oliver Diessel, Guy Gogniat, Mike Hutton, JunKyu Lee, Wayne Luk, Patrick Lysaght, Marco Platzner, Viktor K. Prasanna, Tero Rissa, Cristina Silvano, Hayden Kwok-Hay So, Yu Wang, "**Significant papers from the first 25 years of the FPL conference**", 25th International Conference on Field Programmable Logic and Applications, FPL 2015, London, United Kingdom, September 2-4, 2015, DOI 10.1109/FPL.2015.7293747.
- [E7]. Diana Göhringer, Michael Hübner, Jerónimo Castrillón, Cristina Silvano (**Editors**), ViPES 2015, Preface, 2015 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS) 2015, Samos, Greece, July 19-23, 2015: pp. 347, [DOI](#).
- [E8]. Giovanni Agosta, Cristina Silvano, João M. P. Cardoso, Michael Hübner (**Editors**), Proceedings of the 6th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 4th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms, PARMA-DITAM 2015, Amsterdam, Netherlands, January 21, 2015. ACM 2015, ISBN 978-1-4503-3343-6, [DOI](#).
- [E9]. Cristina Silvano, João M. P. Cardoso, Michael Hübner (**Editors**), Proceedings of the 5th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 3rd Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms, PARMA-DITAM 2014, Vienna, Austria, January 20, 2014. ACM 2014, ISBN 978-1-4503-2607-0, [DOI](#).
- [E10]. Smail Niar and Cristina Silvano (**Guest Co-Editors**), Special Issue DSD 2012 on Reliability and dependability in MPSoC Technologies, Journal on Microprocessors and Microsystems - Embedded Hardware Design, Vol. 37, Number 8-A, 2013, page 759, [DOI](#)
- [E11]. Daniel Gracia Pérez, Smail Niar, Cristina Silvano, Morteza Biglari-Abhari (**Editors**): Proceedings of the 2012 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO '12, 23 January, 2012, Paris, France. ACM 2012, ISBN 978-1-4503-1114-4
- [E12]. Cristina Silvano, Koen Bertels, Michael Schulte (**Guest Co-Editors**), Special Issue with selected papers from International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS2009) on Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), Volume 5, Issue 3, Springer.
- [E13]. Mladen Berekovic; William Fornaciari; Uwe Brinkschulte; Cristina Silvano; (**Editors**), "Architecture of Computing Systems - ARCS 2011", 24th International Conference, Lake Como, Italy, February 24-25, 2011. Proceedings, Springer, Series: Lecture Notes in Computer Science, Vol. 6566, Subseries: Theoretical Computer Science and General Issues, 1st Edition., 2011, XIII, 271 p., ISBN 978-3-642-19136-7.
- [E14]. **Selection Committee Member**, IEEE MICRO Special Issue on "Top Picks 2010 from Computer Architecture Conferences", January/February 2011.
- [E15]. Koen Bertels; Nikita Dimopoulos; Cristina Silvano; Stephan Wong; (**Editors**), Embedded Computer Systems: Architectures, Modeling, and Simulation 9th International Workshop, SAMOS 2009, Samos, Greece, July 20-23, 2009,

Springer Proceedings Series: Lecture Notes in Computer Science Subseries: Theoretical Computer Science and General Issues , Vol. 5657, 2009, XIV, 342 p., Softcover ISBN: 978-3-642-03137-3.

- [E16]. Paolo Faraboschi, Steve Keckler, Antonio Gonzales, Cristina Silvano; (**Editors**) Proceedings of MICRO-41 2008 41st IEEE/ACM International Symposium on Microarchitecture, 2008, 8-12 Nov. 2008, Lake Como.

6.4. CHAPTERS IN INTERNATIONAL BOOKS WITH PEER REVIEW

2016

- [CH1]. Ioannis Stamelakos, Sotirios Xydis, Gianluca Palermo, Cristina Silvano, "Variability-Aware Voltage Island Management for Near-Threshold Computing with Performance Guarantees", pp. 35-53, Near Threshold Computing. Technology, Methods and Applications, Editors: Michael Huebner, Cristina Silvano. Springer, 1st Edition., 2016, IX, 100 p. 56 illus., Hardcover ISBN: 978-3-319-23388-8.

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Milano, November 23rd, 2016

A handwritten signature in black ink, appearing to read 'C. Silvano', written in a cursive style.