Abstract

The demand of digital systems based on CMOS VLSI circuits with low-power features has steadily increased in the scenario of the worldwide microelectronic market. The availability of a suitable hardware/software co-design methodology and related CAD tools is the key issue for the design of complex VLSI-based systems with stringent power and performance requirements. The main purpose of the thesis is the definition of innovative low-power methodologies to support the synthesis and the analysis of digital circuits and systems at the highest abstraction levels and under tight performance constraints. Furthermore, the proposed estimation and optimization techniques are integrated into a hardware/software co-design flow for control-dominated embedded systems. The research activity has been addressed towards two main areas: power estimation and optimization. In fact, power optimization is much more effective when it is tightly integrated with power analysis to make the search for optimal solutions as wide as possible. The first part of the research aims at defining a power assessment framework from a system-level perspective. The main goal is to provide a model to evaluate the power consumption associated with the hardware and software modules as well as the hardware/software communication of a digital system. The second part of the research aims at defining power minimization techniques operating at the system-level. Two main goals have been pursued: the definition of bus encoding schemes for the processor-to-memory communication, and the definition of state assignment algorithms for Finite State Machines. During our research work, a substantial effort has been devoted to demonstrate the effectiveness of the proposed methodologies through their implementation and application to industrial case studies and standard benchmark circuits.