Sample & hold amplifiers
ADC parameters

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Sample & hold amplifiers (SHAs)
Basic SHA scheme

- $R$ is the resistance of the non-ideal switch
- In the ideal case, $h(t - \tau) = \delta(t - \tau)$
Output S/N

• The output noise is
\[ n_{RC}^2 = 4k_B TR \frac{1}{4RC} = \frac{k_B T}{C} \]

• A gate time \( T_G \ll RC \) could be used for fast sampling (gated integrator). The output noise (for unity signal gain) would be
\[ n_{GI}^2 = 4k_B TR \frac{1}{2T_G} \gg n_{RC}^2 \]
Here SHA behaves as an amplifier/follower \(\Rightarrow\) parameters are similar
Pedestal or Hold step

The error is due to parasitic injection through the non-ideal switch

\[ \Delta V \approx \Delta V_{S/H} \frac{C_p}{C_p + C} \]
Aperture time and jitter

From [2]

From [1]
Droop rate

\[ \frac{\Delta V}{\Delta t} = \frac{I_{LKG}}{C_H} \]

\[ I_{LKG} = \text{LEAKAGE CURRENT AT HOLD CAPACITOR, } C_H \]

From [1]
Input feedthrough

\begin{itemize}
  \item Similar to hold step, \( \Delta V \approx V_i C_p / (C_p + C) \)
  \item \( C_p \) can be due to the switch as well as to parasitic layout coupling, ...
\end{itemize}

From [3]
Acquisition time

\[ V_{IN} \rightarrow V_c \]

From [2]
Improved scheme

\[ V_i \rightarrow \text{S/H} \rightarrow C \rightarrow V_o \]
Pros and Cons

• Advantages
  – Impedance decoupling
  – Insensitive to $V_{OS2}$

• Limitations
  – Limited bandwidth owing to the stability requirement when the loop is closed
  – Saturation of the first OPAMP in Hold mode $\Rightarrow$ long acquisition time
Prevention of saturation
SHA with integrator

\[ V_i \rightarrow S/H \rightarrow - \rightarrow + \rightarrow C \rightarrow - \rightarrow + \rightarrow V_o \]
Pros and Cons

• Advantages
  – The S/H switch operates always near zero bias
    • Pedestal error is not input-dependent
    • Input feedthrough during Hold mode is reduced

• Limitations
  – Limited bandwidth owing to the stability requirement when the loop is closed

• Differential architectures with complementary switches can be used to improve performance
ADC DC Parameters
Quantization error

From [4]
Offset or Zero-scale error is the difference between actual and ideal first transition voltage.

Modified from [4]
Offset and dynamic range

Offset leads to a loss in the input range, i.e., a smaller dynamic range

From [5]
Gain and FS errors

- Measured ADC: $y = m_2x + b$
- Gain Error
- Full-Scale Error
- Ideal ADC: $y = (m_1)x$
- Offset Error: $b$

Elettronica 75513  Alessandro Spinelli
DNL

- In an ideal ADC, the transitions are 1 LSB apart
- The difference between the actual and the ideal code width is called DNL
- DNL is measured for each input range or output code; however, only the maximum absolute value is reported
DNL and missing codes

From [4]

\[ V_{REF} = 2.0V \]
Remarks

• If DNL is defined for each output code (see [6]), obviously DNL = -1 ⇒ missing code!

• If DNL is defined for each input range (see [4]), it is always > -1. DNL ≥ 1 does not imply the existence of missing codes

• In any case, |DNL| < 1 ⇒ no missing code!

• If |DNL| ≥ 1 the manufacturer specifies if the ADC has missing codes
• INL is the maximum difference between the real characteristic and an ideal linear behavior

• INL is the sum of DNL errors
Which straight line?

- Offset and gain errors are first removed
- End-point INL is easier and most practical
- Best-fit INL gives lower values but is impractical in most applications
Other parameters...

• Code-edge noise
• Output noise
• Voltage reference specs
  – T drift
  – Voltage noise
  – Long-term stability
  – Load regulation
  – ...

ADC AC Parameters
SNR

- Maximum amplitude of sinusoid is \( A = \frac{V_{ref}}{2} \)
- Signal power
  \[
  \langle V_o^2 \rangle = \langle A^2 \sin^2 \omega t \rangle = \frac{A^2}{2} = \frac{V_{ref}^2}{8} = \frac{2^{2n} \Delta^2}{8}
  \]
- Noise power = quantization noise \( \frac{\Delta^2}{12} \)
  \[
  SNR^2 = \frac{2^{2n} \Delta^2}{8} \cdot \frac{12}{\Delta^2} = \frac{3}{2} \cdot 2^{2n}
  \]
  \[
  SNR_{dB} = 10 \log_{10} \left( \frac{3}{2} \cdot 2^{2n} \right) = 6.02n + 1.76
  \]
SINAD

- If additional noise is present, SNR decreases with respect to the ideal value.
- Another component is (harmonic) distortion.

\[
\text{SINAD} = \frac{\text{rms signal}}{\text{rms (noise + distortion)}} < \text{SNR}
\]

From [7]
SINAD vs. frequency

From [7]

\[ f_s \]
ENOB

- SINAD is expressed as an effective number of bits (ENOB) via the SNR formula

\[
ENOB = \frac{SINAD_{dB} - 1.76}{6.02} < n
\]

- Don’t confuse ENOB with resolution bits
SFDR

From [7]

$$SFDR = \frac{\text{rms signal}}{\text{rms worst spur}}$$

SFDR represents the smallest signal that can be distinguished from a large interference
# ADC technologies

From [8]

<table>
<thead>
<tr>
<th></th>
<th>FLASH (Parallel)</th>
<th>PIPELINE</th>
<th>SAR</th>
<th>SIGMA DELTA</th>
<th>DUAL SLOPE (Integrating)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pick This Architecture if you want:</strong></td>
<td>Ultra-high speed when power consumption not a primary concern</td>
<td>High speeds, few Msps to 100+ Msps, 8 bits to 16 bits, lower power consumption than flash</td>
<td>Medium to high resolution (8 to 16bit), 5Msps and under, low power, small size</td>
<td>High resolution, low to medium speed, no precision external components, simultaneous 50/60Hz rejection, digital filter reduces anti-aliasing requirements</td>
<td>Monitoring DC signals, high resolution, low power consumption, good noise performance</td>
</tr>
<tr>
<td><strong>Conversion Method</strong></td>
<td>N bits – $2^N - 1$ comparators caps increase by a factor of 2 for each bit</td>
<td>Small parallel structure, each stage works on one to a few bits</td>
<td>Binary search algorithm, internal circuitry runs higher speed</td>
<td>Oversampling ADC, 5-Hz – 60 Hz rejection programmable data output</td>
<td>Unknown input voltage is integrated and value compared against known reference value</td>
</tr>
<tr>
<td><strong>Disadvantages</strong></td>
<td>Sparkle codes / metastability, high power consumption, large size, expensive</td>
<td>Parallelism increases throughput at the expense of power and latency</td>
<td>Speed limited to ~5Msps. May require anti-aliasing filter</td>
<td>Higher order (4th order or higher) - multibit ADC and multibit feedback DAC</td>
<td>Slow conversion rate. High precision external components required to achieve accuracy</td>
</tr>
<tr>
<td><strong>Conversion Time</strong></td>
<td>Does not change with increased resolution</td>
<td>Increases linearly with increased resolution</td>
<td>Increases linearly with increased resolution</td>
<td>Tradeoff between data output rate and noise free resolution</td>
<td>Doubles with every bit increase in resolution</td>
</tr>
<tr>
<td><strong>Component Matching Requirements</strong></td>
<td>Typically limits resolution to 8 bits</td>
<td>Double with every bit increase in resolution</td>
<td>Double with every bit increase in resolution</td>
<td>Double with every bit increase in resolution</td>
<td>Does not increase with increase in resolution</td>
</tr>
<tr>
<td><strong>Size</strong></td>
<td>$2^N-1$ comparators, Die size and power increases exponentially with resolution</td>
<td>Die increases linearly with increase in resolution</td>
<td>Die increases linearly with increase in resolution</td>
<td>Core die size will not materially change with increase in resolution</td>
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</tr>
</tbody>
</table>
Resolution and conversion rate

Final choice will depend on application (see discussion in [9])
References