OA parameters

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Slides are supplementary material and are NOT a replacement for textbooks and/or lecture notes.
Outline

• OA datasheets: introduction
• Absolute maximum ratings
• Electrical characteristics
• Typical performance characteristics
Ideal OAs

• Infinite voltage gain
• Infinite bandwidth
• Infinite input impedance
• Zero output impedance
Real OAs – datasheets

ANALOG DEVICES

FEATURES
- Low noise: 30 nV/√Hz at 10 Hz, 3 mV/√Hz
- Low drift: 2 μV/K
- High speed: 2.8 GHz
- High gain bandwidth
- Low Vpp/10 V
- Excellent CMRR, 184 dB at 100 kHz
- High open-loop gain: 1.8 million

GENERAL DESCRIPTION
The OP27/OP27A are high-speed, low-noise, operational amplifier ICs. They operate over a wide supply voltage range and have a rail-to-rail output stage. These features make them suitable for a variety of applications, including imaging, audio, and general-purpose amplification.

OP27

SPECIFICATIONS
ELECTRICAL CHARACTERISTICS

TYPICAL PERFORMANCE CHARACTERISTICS

APPLICATIONS
The OP27/OP27A are ideal for
- Imaging systems
- Audio amplifiers
- General-purpose amplifiers

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Electronics 96032
Datasheet anatomy

• **Features & General description** (sometimes with *Block diagram, Schematic* and *Applications*)
• **Absolute maximum ratings**
• **Electrical characteristics**
• **Typical performance characteristics**
• **Other info (dimensions, package and ordering info, etc.)**
Features/Description

LM158-LM258-LM358

Low power dual operational amplifiers

**Features**
- Internally frequency-compensated
- Large DC voltage gain: 100 dB
- Wide bandwidth (large gain) 1.1 MHz
- Temperature compensated
- Very low supply current per op-amp: essentially independent of supply voltage
- Low input bias current: 20 nA
- Low input offset voltage: 3 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltages
- Large output voltage swing: 8 V

**Applications**
- Linear Technology

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**DESCRIPTION**

These circuits consist of two independent, high-gain, internally frequency-compensated op-amps, which are specifically designed to operate from a single power supply over a wide range of voltages. The low power supply current is independent of the magnitude of the power supply voltage.

Applications include transconductance amplifiers, DC-gain buffers and all the conventional op-amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5 V which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can swing to ground, even though operated from only a single power supply voltage.

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**FEATURES**

- **Voltage Noise**
  - 1.1 mV/√Hz Max at 1 kHz
  - 0.5 mV/√Hz Typ at 1 kHz
  - 1.0 mV/√Hz Typ at 10 kHz
  - 35 mV/√Hz Typ, 0.1 Hz to 10 kHz
- **Voltage and Current Noise**
  - 100% Tested
  - **Gain-Bandwidth Product**
    - **LT1028**: 250 MHz
    - **LT1128**: 150 MHz
- **Slew Rate**
  - **LT1028**: 11 V/μs
  - **LT1128**: 9.5 V/μs
- **Offset Voltage**
  - 40 μV Max
- **Differential Input Voltage Range**
  - 7 V Max
- **Voltage Gain**: 7 M±2 Max
- **Available in 8-Pin SO Package**

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**APPLICATIONS**

- Low Noise/High Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Rate Gyros
- 20Gz Bridge Signal Conditioning
- Magnetic Sensor and Hall
- Microphones
- Tranceiver Transmitters

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**TYPICAL APPLICATION**

[Diagram of typical application]
Outline

• OA datasheets: introduction
• Absolute maximum ratings
• Electrical characteristics
• Typical performance characteristics
Absolute maximum ratings

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>±22 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>±22 V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±7.5 V</td>
</tr>
<tr>
<td>Output Short-Circuit Duration to GND</td>
<td>Indefinite</td>
</tr>
</tbody>
</table>

Storage Temperature Range

- P, S Packages: -65°C to +150°C

Operating Temperature Range

- OP275G: -40°C to +85°C

Junction Temperature Range

- P, S Packages: -65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): 300°C

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_{JA}$</th>
<th>$\theta_{JC}$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead Plastic DIP (P)</td>
<td>103</td>
<td>43</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead SOIC (S)</td>
<td>158</td>
<td>43</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

NOTES

1. Absolute maximum ratings apply to packaged parts, unless otherwise noted.
2. For supply voltages greater than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
3. Shorts to either supply may destroy the device. See data sheet for full details.
4. $\theta_{JA}$ is specified for the worst-case conditions, i.e., $\theta_{JA}$ is specified for device in socket for PDIP packages; $\theta_{JA}$ is specified for device soldered in circuit board for SOIC packages.

AMRs are the maximum values that the OA can safely tolerate. Operation beyond them leads to permanent damage.
Power dissipation

• The increase in junction temperature limits the power dissipation

\[ P_{\text{max}} = \frac{T_{J\text{max}} - T_A}{\theta_{JA}} \]

• Previous example: \( T_{J\text{max}} = 150^\circ\text{C}, \theta_{JA} = 103^\circ\text{C/W} \). For \( T_A = 25^\circ\text{C} \), \( P_{\text{max}} = 1.2 \text{ W} \)

• Power OAs can reach several tens of W
## Operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply voltage</td>
<td>3 to 30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{icm}$</td>
<td>Common mode input voltage range$^{(1)}$</td>
<td>$V_{CC}^\text{-} -0.3$ to $V_{CC}^\text{+} +1.5$</td>
<td>V</td>
</tr>
<tr>
<td>$T_{oper}$</td>
<td>Operating free air temperature range</td>
<td>-55 to +125, -40 to +105, 0 to +70</td>
<td>°C</td>
</tr>
</tbody>
</table>

1. When used in comparator, the functionality is guaranteed as long as at least one input remains within the operating common mode voltage range.

Intervals that guarantee that the OA works as specified
Supply voltage

- Dual symmetrical power supply is almost always used
- Single supply ($+V_{cc}, 0$) can also be used but circuits become a bit more tricky (see later)
Outline

• OA datasheets: introduction
• Absolute maximum ratings
• Electrical characteristics
• Typical performance characteristics
Electrical characteristics

- Show the most important properties of the OA
- Typical, maximum and minimum values at the operating conditions are usually reported
### ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1028AM/AC</th>
<th>LT1028M/C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>( V_{CM} = 0V )</td>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>Long Term Input Offset Voltage Stability</td>
<td></td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>( V_{CM} = 0V )</td>
<td>12</td>
<td>50</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td>( V_{CM} = 0V )</td>
<td>±25</td>
<td>±90</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input Noise Voltage</td>
<td>0.1Hz to 10Hz (Note 4)</td>
<td>35</td>
<td>75</td>
</tr>
</tbody>
</table>

- **Input Noise Voltage Density**
  - $f_D = 10Hz$ (Note 5)
  - $f_D = 1000Hz$, 100% tested
  - 1.00 | 1.7 | 1.0 | 1.9 | nV/√Hz |
  - 0.85 | 1.1 | 0.9 | 1.2 | nV/√Hz |

- **Input Noise Current Density**
  - $f_D = 10Hz$ (Note 4 and 6)
  - $f_D = 1000Hz$, 100% tested
  - 4.7 | 10.0 | 4.7 | 12.0 | pA/√Hz |
  - 1.0 | 1.8 | 1.0 | 1.8 | pA/√Hz |

- **Input Resistance**
  - Common Mode
  - Differential Mode
  - 300 | 300 | MΩ |
  - 20 | 20 | kΩ |

- **Input Capacitance**
  - 5 | 5 | pF |

- **Input Voltage Range**
  - \( \pm 11.0 \) | \( \pm 12.2 \) | \( \pm 11.0 \) | \( \pm 12.2 \) | V |

- **CMRR** Common Mode Rejection Ratio
  - \( V_{CM} = \pm 11V \)
  - 114 | 126 | 110 | 126 | dB |

- **PSRR** Power Supply Rejection Ratio
  - \( V_S = \pm 4V \) to \( \pm 18V \)
  - 117 | 133 | 110 | 132 | dB |

- **AVOL** Large-Signal Voltage Gain
  - \( R_L > 2k \), \( V_O > \pm 12V \)
  - \( R_L > 1k \), \( V_O > \pm 10V \)
  - \( R_L > 600Ω \), \( V_O > \pm 10V \)
  - 7.0 | 30.0 | 5.0 | 30.0 | V/V |
  - 5.0 | 20.0 | 3.5 | 20.0 | V/V |
  - 3.0 | 15.0 | 2.0 | 15.0 | V/V |

- **VOUT** Maximum Output Voltage Swing
  - \( R_L > 2k \)
  - \( R_L > 600Ω \)
  - \( +11.0 \) | \( +12.2 \) | \( +10.5 \) | \( +12.2 \) | V |

- **SR** Slew Rate
  - \( A_{VOL} = -1 \)
  - \( A_{VOL} = -1 \)
  - \( \text{LT1028} \)
  - \( \text{LT1128} \)
  - 11.0 | 15.0 | 11.0 | 15.0 | V/µs |
  - 5.0 | 6.0 | 4.5 | 6.0 | V/µs |

- **GBW** Gain-Bandwidth Product
  - \( f_O = 20kHz \) (Note 7)
  - \( f_O = 10kHz \) (Note 7)
  - \( f_O = 20kHz \)
  - \( f_O = 10kHz \)
  - \( \text{LT1028} \)
  - \( \text{LT1128} \)
  - 50 | 75 | 50 | 75 | MHz |
  - 13 | 20 | 11 | 20 | MHz |

- **Z_o** Open-Loop Output Impedance
  - \( V_O = 0 \), \( I_O = 0 \)
  - 80 | 80 | Ω |

- **I_S** Supply Current
  - 7.4 | 9.5 | 7.6 | 10.5 | mA |
I/O voltage ranges

A common-mode input range is also defined, related to $(V^+ + V^-)/2$
Large-signal voltage gain

- $A_V$ is the slope of the linear interpolation
- Typ. 80 – 120 dB, depending on $V_{cc}, R_L, T,$...
• Typ. 1-5 mV; precision OAs have $V_{OS} < 0.5$ mV
• Due to mismatch of the input transistors
$V_{OS}$ representation

- Best BJT OA: $10 - 25 \mu V$
- Best JFET OA: $100 \mu V - 1 mV$
- Best CMOS OA: $< 100 \mu V - 1 mV$
Offset voltage drift

- Is the temperature dependence of $V_{OS}$
- Typical values for general-purpose OA is $1 - 10 \, \mu V/°C$
- Low-drift OA have $dV_{OS}/dT < 0.3 \, \mu V/°C$

- «Chopper-stabilized» or «auto-zero» OA feature $V_{OS} < 1 \, \mu V$ and $dV_{OS}/dT < 30 \, nV/°C$
  (more on this at the end of the course)
Input bias current

- BJTs in input stage require a DC base current $I_b$
- JFETs as input devices have reverse-biased $p$-$n$ junctions
- MOSFETs have ESD protection circuits (diodes) which determine $I_b$
$I_b$ representation

- Typ. BJT OA: $10^{-8} - 10^{-6}$ A
- Typ. JFET OA: $10^{-13} - 10^{-10}$ A
- Typ. CMOS OA: $10^{-13} - 10^{-10}$ A (ESD circ.)
Input offset current

• Bias currents at the two inputs are actually different, $I_b^+$ and $I_b^-$

• $I_b$ is defined as their average value

• Offset current is defined as $I_{OS} = |I_b^+ - I_b^-|$

• Usually, an order of magnitude smaller than $I_b$
$I_b$ and $I_{OS}$ drift

- In FET and CMOS OAs, $I_b$ and $I_{OS}$ increase by a factor of two every $10^\circ C$ (reverse currents of $p$-$n$ junctions) $\Rightarrow$ check $T$ range if low current is needed!

- BJT OAs usually have lower drifts (10 – 100 pA/$^\circ C$)
Offset compensation

Detailed compensation scheme provided by manufacturer
Offset compensation (DIY)
If $R = R_1 \parallel R_2$, $I_b$ is compensated and

$$V_o = I_b R_2 - I_b^+ R \left( \frac{R_1 + R_2}{R_1} \right)$$

$$= I_b R_2 \left( 1 - \frac{R}{R_1 \parallel R_2} \right)$$

$$+ I_{OS} \frac{R_2}{2} \left( 1 + \frac{R}{R_1 \parallel R_2} \right)$$

$$V_o = I_{OS} R_2 \quad \text{(only useful if } I_{OS} \ll I_b)$$
Remarks

- Carefully pick compensation resistor values in order not to alter the gain.
- Obviously, drift or long-term stability cannot be compensated this way!
Total error – inverting amplifier

\[ V_o = -\frac{R_2}{R_1} \left( V_i + V_{OS} \frac{R_1 + R_2}{R_2} + I_{OS}R_1 \right) \]

Error (trade-off with \( R_{in} = R_1 \))
Total error – non-inverting amplifier

\[ V_o = \frac{R_1 + R_2}{R_1} (V_i + V_{OS} + I_{OS} \frac{R_1}{R_2}) \]
Input resistance

- Usually $R_c \gg R_d$
- An input capacitance of a few pF must also be considered at high frequencies

- Typ. BJT OA: $10^6 - 10^8 \Omega$
- Typ. JFET OA: $10^9 - 10^{10} \Omega$
- Typ. CMOS OA: $10^{12} \Omega$
Output resistance

- Typically smaller than 100 Ω
- A bit higher in CMOS OA
Common and differential modes

- Given the input voltages $V^+$ and $V^-$, we define
  - Common-mode voltage $V_c = \frac{V^+ + V^-}{2}$
  - Differential-mode voltage $V_d = V^+ - V^-$
Common mode rejection ratio

• The OA output is given by

\[ V_o = A_d V_d + A_c V_c = A_d \left( V_d + \frac{A_c}{A_d} V_c \right) = \]

\[ = A_d \left( V_d + \frac{V_c}{CMRR} \right) \]

where

\[ CMRR = \frac{A_d}{A_c} \]

• Typical values are 70 – 120 dB
Power supply rejection ratio

• PSRR is the ratio between the PS disturbs and the differential signal that gives the same output

• Typical values are 80 – 100 dB
Gain-bandwidth product

- Open-loop gain can usually be expressed as
  \[ A(s) = \frac{A_0}{1 + s\tau} \]

- \( GBWP \) is the unity-gain frequency
  \[ GBWP = \frac{A_0}{2\pi\tau} \]
Internal circuit (block scheme)

- **Input stage** (gm)
  - [Diagram showing the input stage components]
- **Gain stage**
  - [Diagram showing the gain stage components]
- **Output stage** (unity gain)
  - [Diagram showing the output stage components]

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Slew rate

Typical values are 1 V/µs — 100 V/µs or more
Full-power Bandwidth

\[ V_o = V_M \sin(\omega t) \]
\[ \frac{dV_o}{dt}\bigg|_{max} = \omega V_M < SR \]

• The OA can work at the maximum swing, \( V_o^{max} \), without being limited by \( SR \) if

\[ f \leq \frac{SR}{2\pi V_o^{max}} = FPBW \]
Outline

• OA datasheets: introduction
• Absolute maximum ratings
• Electrical characteristics
• Typical performance characteristics
Typical performance characteristics

• Show actual data for the different parameters
• Basic data are always reported, but there is no standard ⇒ every manufacturer specifies what he thinks are the most important dependences
I/O voltage swing

Non-symmetrical
Voltage gain

(low-power CMOS OA)
Offset voltage and drift

BJT, precision

JFET
Bias current

- BJT
- JFET
- CMOS

Exponential dependence!
Extremely low $I_b$

- LMP 7721 and INA 116 (other models may exist): $I_b \approx 3$ fA typ., $\approx 20$ fA max
- Offset currents are comparable to $I_b$
- Achieved with bias-cancellation circuitry
Open-loop output impedance

Power OA
CMRR and PSRR decrease with frequency
GBWP

- Gain Bandwidth vs. Temperature
- Phase Margin vs. Temperature
- Gain Bandwidth vs. Supply Voltage

**Curves:**
- $V_S = \pm 10\,V$
- $V_S = \pm 15\,V$
- $V_S = \pm 20\,V$

**Parameters:**
- $\phi_m$
- $R_L = 2\,k$
Slew rate

Graphs showing the relationship between slew rate and temperature, gain-bandwidth product, and differential input voltage.
Full-power bandwidth

$$2\pi f V_o = SR$$

$$FPBW = \frac{SR}{2\pi V_o^{max}}$$
Small-signal response

SR limits

Rise/fall times are sometimes specified
Conclusions

• Datasheets provide an extensive characterization of the OA behavior

• Not all data should be considered: always check what your application requires and choose the OA that better suits your needs